

**BOARD ROUTING RECOMMENDATIONS** 

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#### 4.0 PIN ASSIGNMENTS



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# molex®

### **PCIE 16X CONNECTOR**

#### **BOARD ROUTING RECOMMENDATIONS**

#### 1.0 SCOPE

This specification covers the PCle X16, 0.80mm centerline connector and the high-speed PCB routing recommendations. The connector is a dual paddle card assembly. There are sixteen sets of differential pairs, eight on each paddle card. The connector has 136 contacts of which 48 can be assigned to high speed differential signal pairs and at least 64 are for ground terminals. The connector is a right angle press-fit compliant pin type designed for use with 0.46mm finished vias for the signal pins.

The connector has compliant pin contacts for mechanical retention to the PC board. The connector provides outer electromagnetic interference (EMI) suppression with an elastomeric EMI gasket that contacts the panel. The connector assembly is designed to be inserted through a standard bezel after being seated onto the PC board.

See Figure 1 below.

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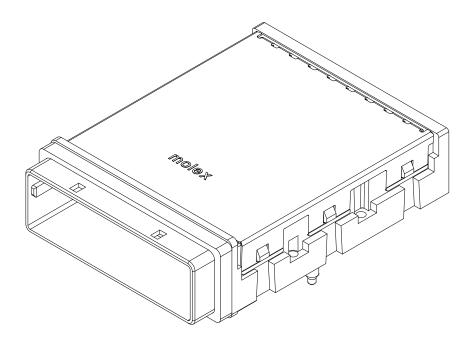


Figure 1

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#### **BOARD ROUTING RECOMMENDATIONS**

#### 2.0 PC BOARD REQUIREMENTS

#### **MATERIAL THICKNESS**

The recommended minimum pc board thickness shall be 1.35 mm. Suitable pc board material shall be glass epoxy (FR-4 or G-10).

#### 2.2 TOLERANCE

Maximum allowable bow of the pc board shall be 0.08 mm over the length of the connector assembly.

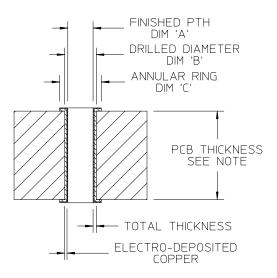
#### 2.3 HOLE DIMENSIONS

The holes for the connector assembly must be drilled and plated through to dimensions specified in Figure 2.

#### 2.4 LAYOUT

The holes for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Recommended hole pattern, dimensions, and tolerances are provided in Figure 3.

#### Recommended Hole Dimensions



DIM. "A"	DIM. "B"	DIM. "C"
MM / (INCH)	MM / (INCH) - # DRILL	MM / (INCH)
1.05+/-0.05 (.0413+/002)	1.181 (.0465) - # 56	1.40 (.055)
0.81+/-0.05 (.032+/002)	0.711 (.028) - # 70	1.16 (.046)
0.57+/-0.05 (.022+/002)	0.66 (0.260) - # 71	0.91 (.036)
0.46+/-0.05 (.0181+/002)	0.572 (.022) - # 74	0.81 (.032)
0.37+/-0.05 (.0146+/002)	0.457 (.018) - # 77	0.72 (.028)

Note: Refer to appropriate sales drawing for recommended pcb holes and pcb thickness.

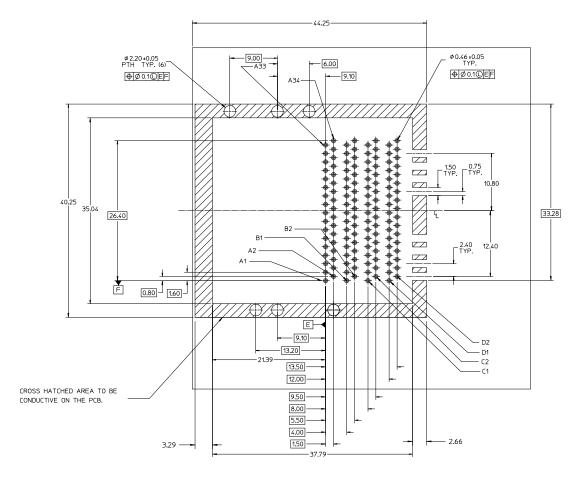
### PLATING DETAIL FOR 0.37MM DIA. COMPLIANT PIN HOLES

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**BOARD ROUTING RECOMMENDATIONS** 

# Figure 2 Recommended PC Board Layout for the Connector Assembly Connector



Pattern Detail **Figure 3** 

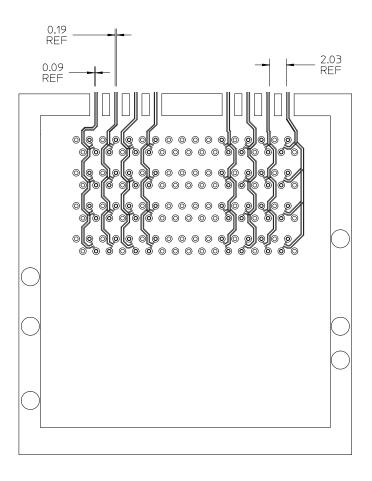
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**BOARD ROUTING RECOMMENDATIONS** 

### 3.0 HIGH-SPEED ROUTING

#### 3.1 GENERAL 2X3 ROUTING EXAMPLE



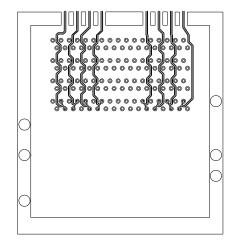
Showing 4 layer overlaid for a 16x configuration Routing example shown for reference only.

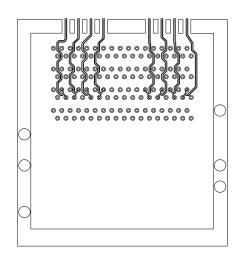
Shown with 0.0889mm (0. 0035") traces and 0.1905mm (0.0075") spaces 2.0317 (0.0799") spaces between pair traces.

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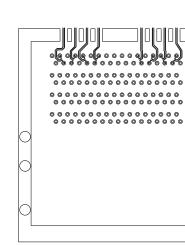


### **BOARD ROUTING RECOMMENDATIONS**

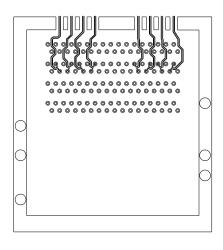




1<sup>ST</sup> LAYER







3<sup>RD</sup> LAYER

4TH LAYER

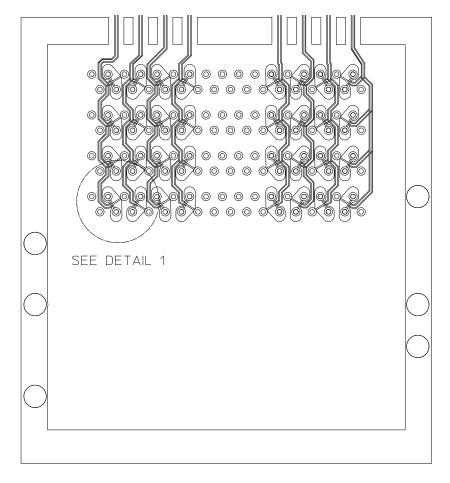
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**BOARD ROUTING RECOMMENDATIONS** 

### 3.2 HIGH-SPEED TRANSMISSION LINE PLANE



Showing 4 layers overlaid for a typical single connector

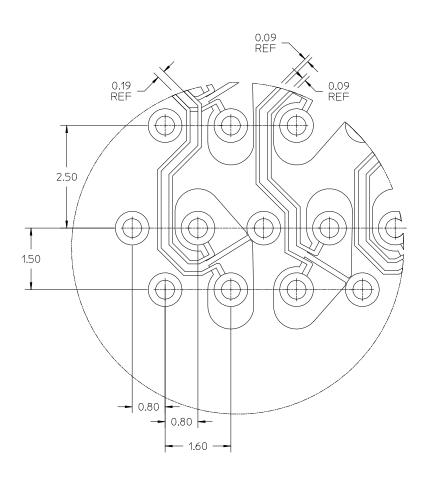
Reference ground layer shown and spacing between trace pairs Routing example shown for reference only

Shown with 0.0889mm (0. 0035") traces and 0.1905mm (0.0075") spaces 2.0317 (0.0799") spaces between pair traces.

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**BOARD ROUTING RECOMMENDATIONS** 



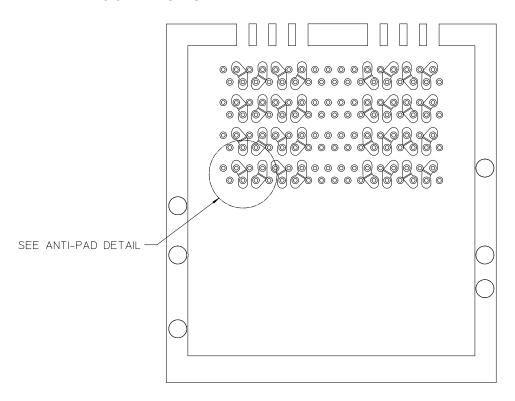
Trace detail typical for all trace positions

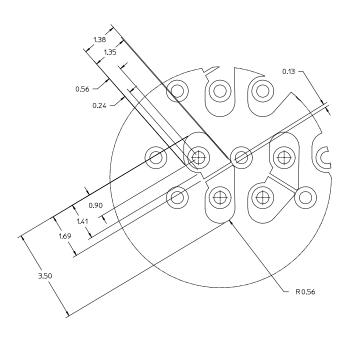
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**BOARD ROUTING RECOMMENDATIONS** 

### 3.3 HIGH-SPEED REFERENCE PLANE ANTI-PAD





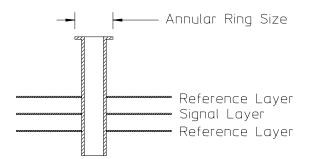
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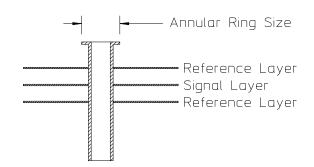


**BOARD ROUTING RECOMMENDATIONS** 

### **Signal Ground Planes**

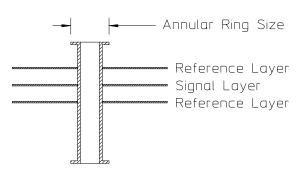
#### 3.4 CONNECTOR PRESS-FIT INTERFACE VIA STUBS

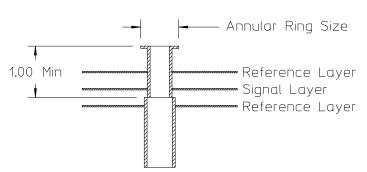




### BOTTOM LAUNCH DRIVEN VIA (PREFERRED)

TOP LAUNCH STUB VIA (WORSE CASE)





**BACK DRILLED 1.00MM MAX FROM TOP** 

#### STANDARD VIA CONFIGURATION

Only two annular rings are required for retention of the press-fit via within the printed circuit consequently annular rings on the bottom layer are not needed. Removing the bottom layer annular ring helps minimize the parasitic stub capacitance created by the via.

The anti-pad can be used on other ground layers not shown above. Alternatively, the anti-pad can be made larger with a broader keep-out region on these other ground layers to minimize parasitic capacitance.

For the connector press-fit vias, specify not only the 0.37mm (0.014") finished hole size but also the 0.45715mm (0.018") drill size for the board fabrication.

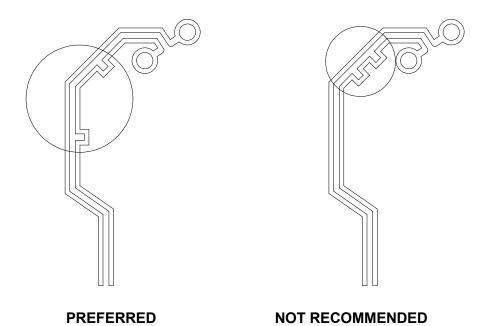
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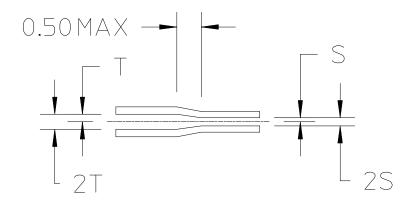
**BOARD ROUTING RECOMMENDATIONS** 

#### **SKEW COMPENSATION** 3.5



It is recommended that skew compensation be distributed verses grouped in one or more locations.

#### 3.6 TRACE COMPARISON



### TRANSITION SHOULD BE SYMETRIC

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### **BOARD ROUTING RECOMMENDATIONS**

### 4.0 Pin Assignments

Notes:

- See sheet no. 4 for physical locations of pin assignments
   Reference PCI EXPRESS EXTERNAL CABLING SPECIFICATION, Rev.1.0 for further details

### 1<sup>st</sup> Row

Pin	Symbol	Description	Pin	Symbol	Description
A1	GND	Ground	A34	RSVD	Reserved
A2	PERp1	Differential PCI Express Receiver	A33	GND	Ground
	r	Lane 1	A32	PERn15	Differential PCI Express Receiver
A3	PERn1	Differential PCI Express Receiver			Lane 15
		Lane 1	A31	PERp15	Differential PCI Express Receiver
A4	GND	Ground			Lane 15
A5	PERp3	Differential PCI Express Receiver	A30	GND	Ground
		Lane 3	A29	PERn13	Differential PCI Express Receiver
A6	PERn3	Differential PCI Express Receiver			Lane 13
		Lane 3	A28	PERp13	Differential PCI Express Receiver
A7	GND	Ground			Lane 13
A8	PERp5	Differential PCI Express Receiver	A27	GND	Ground
		Lane 5	A26	PERn11	Differential PCI Express Receiver
A9	PERn5	Differential PCI Express Receiver			Lane 11
		Lane 5	A25	PERp11	Differential PCI Express Receiver
A10	GND	Ground			Lane 11
A11	PERp7	Differential PCI Express Receiver	A24	GND	Ground
		Lane 7	A23	PERn9	Differential PCI Express Receiver
A12	PERn7	Differential PCI Express Receiver			Lane 9
		Lane 7	A22	PERp9	Differential PCI Express Receiver
A13	GND	Ground			Lane 9
A14	PWR	+3.3 V Power (Optional)	A21	GND	Ground
A15	PWR	+3.3 V Power (Optional)	A20	uREFCLKn	Differential 100MHz Cable
A16	PWR	+3.3 V Power (Optional)			Reference Clock at Upstream
A17	uSB_RTN	Signal Return for Single Ended			Subsystem
		Sideband Signals (GND)			
A18	GND	Ground			
A19	uREFCLKp	Differential 100MHz Cable			
		Reference Clock at Upstream			
	1	Subsystem	- 1		

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### **BOARD ROUTING RECOMMENDATIONS**

### 2<sup>nd</sup> Row

Pin	Symbol	Description
B1	GND	Ground
B2	PERp0	Differential PCI Express Receiver
		Lane 0
В3	PERn0	Differential PCI Express Receiver
		Lane 0
B4	GND	Ground
B5	PERp2	Differential PCI Express Receiver
		Lane 2
В6	PERn2	Differential PCI Express Receiver
		Lane 2
B7	GND	Ground
B8	PERp4	Differential PCI Express Receiver
		Lane 4
B9	PERn4	Differential PCI Express Receiver
		Lane 4
B10	GND	Ground
B11	PERp6	Differential PCI Express Receiver
		Lane 6
B12	PERn6	Differential PCI Express Receiver
		Lane 6
B13	GND	Ground
B14	PWR_RTN	Return for +3.3 V Power (Optional)
B15	PWR_RTN	Return for +3.3 V Power (Optional)
B16	PWR_RTN	Return for +3.3 V Power (Optional)
B17	uPWRON	Power Valid Notification at
		Upstream Subsystem
B18	uWAKE#	Power Management Signal for
		Wakeup Events (Optional)
B19	uPRSNT#	Used for Detection if a Cable is
		Installed

Pin	Symbol	Description
B34	RSVD	Reserved
B33	GND	Ground
B32	PERn14	Differential PCI Express Receiver Lane 14
B31	PERp14	Differential PCI Express Receiver Lane 14
B30	GND	Ground
B29	PERn12	Differential PCI Express Receiver Lane 12
B28	PERp12	Differential PCI Express Receiver Lane 12
B27	GND	Ground
B26	PERn10	Differential PCI Express Receiver Lane 10
B25	PERp10	Differential PCI Express Receiver Lane 10
B24	GND	Ground
B23	PERn8	Differential PCI Express Receiver Lane 8
B22	PERp8	Differential PCI Express Receiver Lane 8
B21	GND	Ground
B20	uPERST#	Cable PERST# at Upstream Subsystem

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### **BOARD ROUTING RECOMMENDATIONS**

### 3<sup>rd</sup> Row

Pin	Symbol	Description	Pin	Symbol	Description
C1	GND	Ground	C34	RSVD	Reserved
C2	PETp1	Differential PCI Express Transmitter	C33	GND	Ground
	-	Lane 1	C32	PETn15	Differential PCI Express Transmitter
C3	PETn1	Differential PCI Express Transmitter			Lane 15
		Lane 1	C31	PETp15	Differential PCI Express Transmitter
C4	GND	Ground			Lane 15
C5	PETp3	Differential PCI Express Transmitter	C30	GND	Ground
		Lane 3	C29	PETn13	Differential PCI Express Transmitter
C6	PETn3	Differential PCI Express Transmitter			Lane 13
		Lane 3	C28	PETp13	Differential PCI Express Transmitter
C7	GND	Ground			Lane 13
C8	PETp5	Differential PCI Express Transmitter	C27	GND	Ground
		Lane 5	C26	PETn11	Differential PCI Express Transmitter
C9	PETn5	Differential PCI Express Transmitter		DET 11	Lane 11
0.10	OVE	Lane 5	C25	PETp11	Differential PCI Express Transmitter
C10	GND	Ground		OND	Lane 11
C11	PETp7	Differential PCI Express Transmitter	C24	GND	Ground
0.10	DET 7	Lane 7	C23	PETn9	Differential PCI Express Transmitter
C12	PETn7	Differential PCI Express Transmitter		DET 0	Lane 9
040	OND	Lane 7	C22	PETp9	Differential PCI Express Transmitter
C13	GND	Ground	-004	OND	Lane 9
C14	PWR	+3.3 V Power (Optional)	C21	GND	Ground
C15	PWR	+3.3 V Power (Optional)	C20	dREFCLKn	Differential 100MHz Cable
C16	PWR	+3.3 V Power (Optional)	4		Reference Clock at Downstream
C17	dSB_RTN	Signal Return for Single Ended	<u> </u>	1	Subsystem
0.10	OUD	Signals at Downstream Subsystem	4		
C18	GND	Ground	4		
C19	dREFCLKp	Differential 100MHz Cable			
		Reference Clock at Downstream			
		Subsystem			

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### **BOARD ROUTING RECOMMENDATIONS**

### 4<sup>th</sup> Row

Pin	Symbol	Description
D1	GND	Ground
D2	PETp0	Differential PCI Express Transmitter
		Lane 0
D3	PETn0	Differential PCI Express Transmitter
		Lane 0
D4	GND	Ground
D5	PETp2	Differential PCI Express Transmitter
		Lane 2
D6	PETn2	Differential PCI Express Transmitter
		Lane 2
D7	GND	Ground
D8	PETp4	Differential PCI Express Transmitter
		Lane 4
D9	PETn4	Differential PCI Express Transmitter
		Lane 4
D10	GND	Ground
D11	PETp6	Differential PCI Express Transmitter
		Lane 6
D12	PETn6	Differential PCI Express Transmitter
5.40	0115	Lane 6
D13	GND	Ground
D14	PWR_RTN	Return for +3.3 V Power (Optional)
D15	PWR_RTN	Return for +3.3 V Power (Optional)
D16	PWR_RTN	Return for +3.3 V Power (Optional)
D17	dPWRON	Power Valid Notification
D18	dWAKE#	Power Management for Wakeup
		Events at Downstream Subsystem
D19	dPRSNT#	Used for Detection if a Cable is
		Installed

Pin	Symbol	Description
D34	RSVD	Reserved
D33	GND	Ground
D32	PETn14	Differential PCI Express Transmitter
		Lane 14
D31	PETp14	Differential PCI Express Transmitter
		Lane 14
D30	GND	Ground
D29	PETn12	Differential PCI Express Transmitter
		Lane 12
D28	PETp12	Differential PCI Express Transmitter
		Lane 12
D27	GND	Ground
D26	PETn10	Differential PCI Express Transmitter
		Lane 10
D25	PETp10	Differential PCI Express Transmitter
		Lane 10
D24	GND	Ground
D23	PETn8	Differential PCI Express Transmitter
		Lane 8
D22	PETp8	Differential PCI Express Transmitter
		Lane 8
D21	GND	Ground
D20	dPERST#	Cable PERST# at Downstream
		Subsystem

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