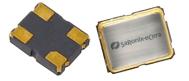


FK Series Crystal Clock Oscillator (XO) 3.2 x 2.5mm

2.5V CMOS Low Jitter XO





3.2 x 2.5mm Ceramic SMD

Product Features

- •1 to 156.25 MHz Frequency Range
- •<1 ps RMS jitter
- •2.5V CMOS compatible logic levels
- Designed for standard reflow and washing techniques
- Low power standby mode
- Pb-free and RoHS/Green compliant

Product Description

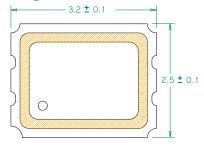
The FK Series 2.5V crystal clock oscillator achieves superb stability and low power consumption over a broad range of operating conditions and frequencies. The low jitter output clock signal, generated internally with a non-PLL oscillator design, is compatible with LVCMOS logic levels. The device, available on tape and reel, is contained in a 3.2 x 2.5mm surface-mount ceramic package.

Applications

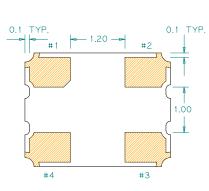
Ideal for compact, high-density applications requiring low power or tight stability, including:

- Network adapter cards
- Portable Multimedia Devices
- Hard Disk Drives
- •GPS/Navigation
- Bluetooth
- •802.11a/b/g WiFi

Package:







Recommended Land Pattern: $2.12 \rightarrow$ $4 \qquad 43 \qquad 1.6$ $1.2 \quad TYP.$ $4 \qquad 1.5 \quad TYP.$

Pin Functions:

Pin	Function					
1	OE					
2	Ground					
3	Clock Output					
4	V _{DD}					

Part Ordering Information:

FK XXX YYYY



Following the above format, Saronix-eCera part numbers will be assigned upon confirmation of exact customer requirements.

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15-0087

SaRonix-eCera

FK Series Crystal Clock Oscillator (XO) 3.2 x 2.5mm

Electrical Performance

Parameter		Min.	Тур.	Max.	Units	Notes
Output Frequen	cy	1		156.25	MHz	As specified
Supply Voltage		2.25	2.5	2.75	V	
Supply Current, Output Enabled				10	mA	1 to 50 MHz
				18	mA	50 to 156.25 MHz
Supply Current, Standby Mode				10	μΑ	Output Hi-Z
Frequency Stability				±20 to ±50	ppm	See Note 1 below
Operating Temperature Range		-20		+70	°C	Commercial (standard)
		-40		+85	C	Industrial (standard)
Output Logic 0, V _{OL}				10% V _{DD}	V	
Output Logic 1, V _{OH}		90% V _{DD}			V	
Output Load	Output Load			15	pF	
Duty Cycle	Duty Cycle			55	%	Measured 50% V _{DD}
Rise and Fall Ti	Rise and Fall Time			5	ns	Measured 10/90% of waveform
Jitter, Phase	1 to 156.25 MHz			1	ps RMS (1-σ)	12kHz to 20 MHz frequency band
Jitter, Accumulated	up to 75 MHz			5	$\mathbf{p} \in \mathbf{DMS}(1, \mathbf{r})$	20.000 adjacent periods
	75 to 156.25 MHz			3	ps RMS (1-σ)	
Jitter, Total	up to 75 MHz			50	na nk nk	100,000 random parioda
	75 to 156.25 MHz			30	ps pk-pk	100.000 random periods

Notes:

1. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C),

aging (1 year at 25°C average effective ambient temperature), shock and vibration.

2. For specifications othere than those listed, please contact sales.

Output Enable / Disable Function

Parameter	Min.	Тур.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	0.7 V _{DD}			V	or open
Input Voltage (pin 1), Output Disable (low power standby)			0.3 V _{DD}	V	Output is Hi-Z
Internal pullup resistance	50			kΩ	
Output Disable Delay			100	ns	
Output Enable Delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Тур.	Max.	Units	Notes
Storage Temperature	-55		+125	°C	

For the latest product information visit: http://www.pericom.com/products/timing/oscillators/FK2.5/

For test circuit go to: http://www.pericom.com/pdf/sre/tc_hcmos2.pdf

For soldering reflow profile and reliability test ratings go to: <u>http://www.pericom.com/pdf/sre/reflow.pdf</u>

For tape and reel information go to: http://www.pericom.com/pdf/sre/tr_3225_xo.pdf

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