Document Number: AFT21H350W03S
Rev. 0, 9/2013

RoHS

RF Power LDMOS Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

These 63 watt asymmetrical Doherty RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2170 MHz.

- Typical Doherty Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 750 mA, V_{GSB} = 0.7 Vdc, P_{out} = 63 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

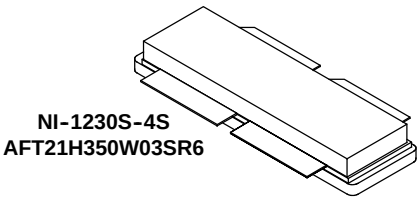
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	16.4	47.1	7.5	–26.0
2140 MHz	16.5	46.3	7.5	–27.9
2170 MHz	16.5	45.2	7.4	–30.1

Features

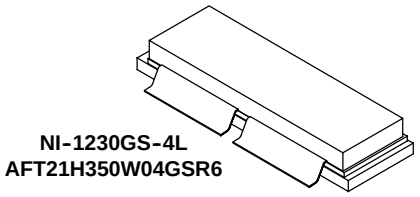
- Advanced High Performance In–Package Doherty
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13–inch Reel.

AFT21H350W03SR6
AFT21H350W04GSR6

2110–2170 MHz, 63 W AVG., 28 V
AIRFAST RF POWER LDMOS TRANSISTORS



NI–1230S–4S
AFT21H350W03SR6



NI–1230GS–4L
AFT21H350W04GSR6

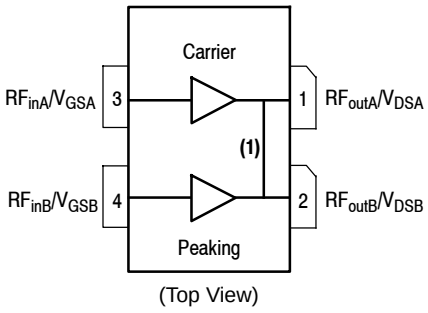


Figure 1. Pin Connections

1. Pin connections 1 and 2 are DC coupled and RF independent.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	−0.5, +65	Vdc
Gate−Source Voltage	V_{GS}	−6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	−40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	324 0.79	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 79°C, 63 W CW, 28 Vdc, I_{DQA} = 750 mA, V_{GSB} = 0.7 Vdc, 2140 MHz	$R_{\theta JC}$	0.49	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22−A114)	2
Machine Model (per EIA/JESD22−A115)	B
Charge Device Model (per JESD22−C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate−Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics − Side A (Carrier)					
Gate Threshold Voltage (5) (V_{DS} = 6 Vdc, I_D = 146 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (5) (V_{DD} = 28 Vdc, I_{DA} = 750 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain−Source On−Voltage (4) (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics − Side B (Peaking)					
Gate Threshold Voltage (5) (V_{DS} = 6 Vdc, I_D = 303 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain−Source On−Voltage (4) (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

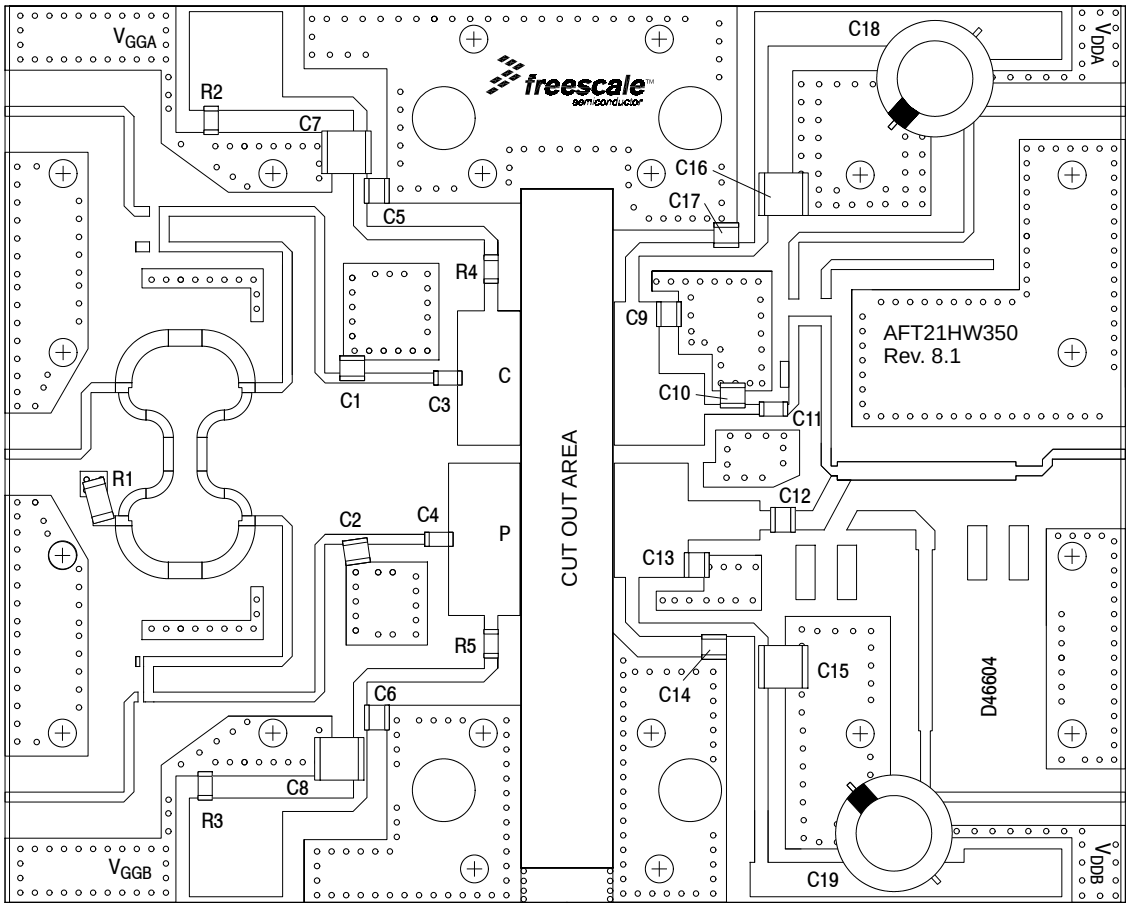
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1955
4. Side A and Side B are tied together for these measurements.
5. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 750 mA, V_{GSB} = 0.7 Vdc, P_{out} = 63 W Avg., f = 2110 MHz, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	15.5	16.4	18.5	dB
Drain Efficiency	η_D	43.6	47.1	—	%
Output Peak−to−Average Ratio @ 0.01% Probability on CCDF	PAR	7.0	7.5	—	dB
Adjacent Channel Power Ratio	ACPR	—	−26.0	−24.1	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 750 mA, f = 2140 MHz					
VSWR 10:1 at 32 Vdc, 195 W CW Output Power (3 dB Input Overdrive from 110 W CW Rated Power)	No Device Degradation				
Typical Performances (3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 750 mA, V_{GSB} = 0.7 Vdc, 2110−2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	110	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	400	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110 to 2170 MHz frequency range)	Φ	—	40	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	140	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 63 W Avg.	G_F	—	0.4	—	dB
Gain Variation over Temperature (−30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (−30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

1. V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurements made with device in an asymmetrical Doherty configuration.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W−CDMA single−carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. AFT21H350W03SR6 Test Circuit Component Layout

Table 5. AFT21H350W03SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C2	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
C3, C4, C11, C12	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C5, C6, C14, C17	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C7, C8, C15, C16	10 μF Chip Capacitors	GRM55DR61H106KA88L	Murata
C9	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C10, C13	0.8 pF Chip Capacitors	ATC100B0R8BT500XT	ATC
C18, C19	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1	51 Ω, 1/2 W Chip Resistor	CRCW201051R0JNEF	Vishay
R2, R3	3.0 KΩ, 1/4 W Chip Resistors	CRCW12063K00FKEA	Vishay
R4, R5	2.7 Ω, 1/4 W Chip Resistors	CRCW12062R70FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.5	D46604	MTL

TYPICAL CHARACTERISTICS

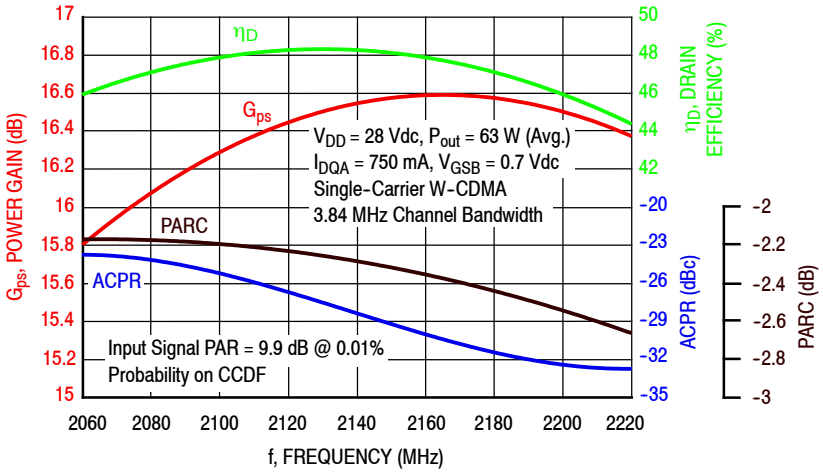


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

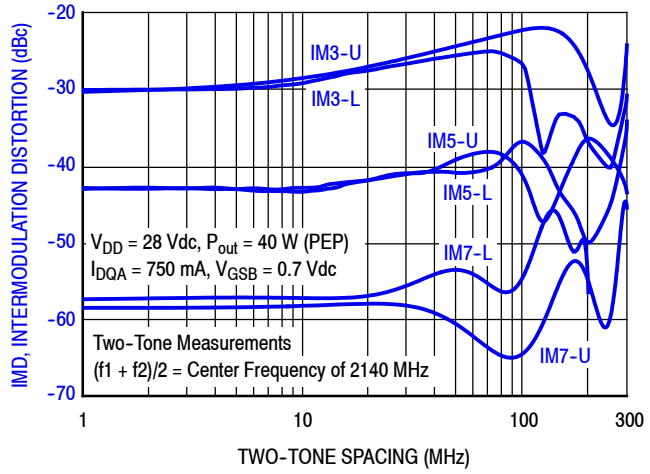


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

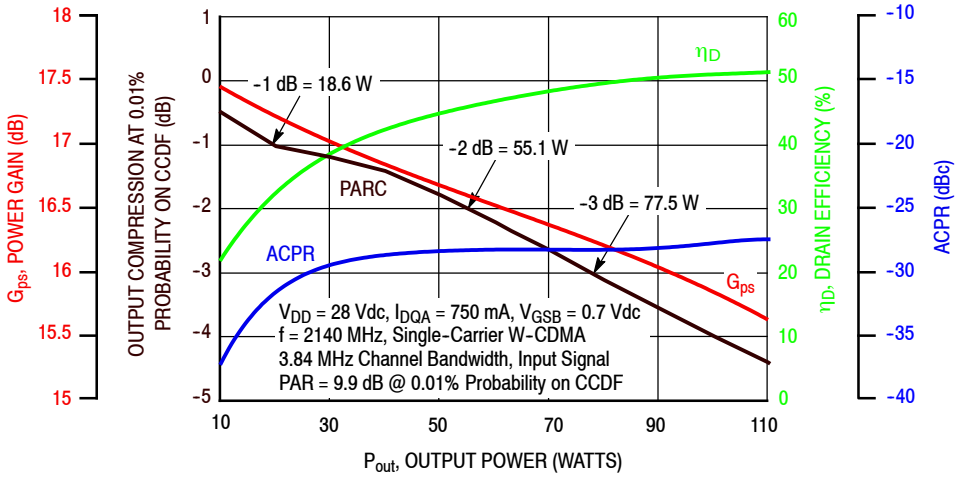


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

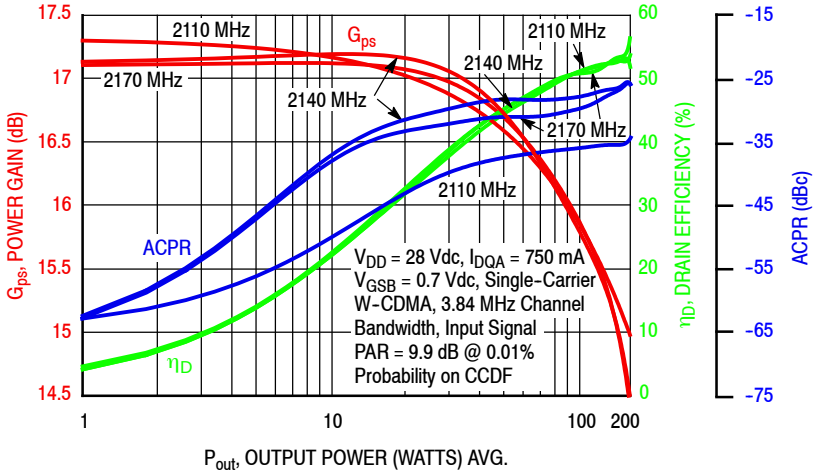


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

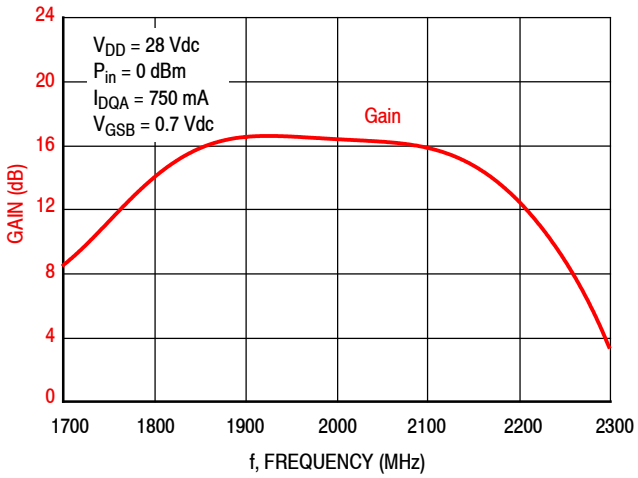


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 763 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.29 - j7.28	3.75 + j6.90	3.07 - j4.95	18.7	51.9	155	54.7	-12
2140	5.23 - j7.74	4.64 + j7.21	3.16 - j5.18	18.7	51.9	156	54.8	-13
2170	6.26 - j7.95	5.75 + j7.35	3.27 - j5.37	18.9	51.9	155	54.1	-13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.29 - j7.28	3.96 + j7.42	3.18 - j5.59	16.5	52.8	189	57.1	-18
2140	5.23 - j7.74	5.04 + j7.81	3.30 - j5.71	16.6	52.8	189	56.8	-19
2170	6.26 - j7.95	6.44 + j7.94	3.40 - j5.88	16.7	52.7	187	56.2	-20

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Carrier Side Load Pull Performance — Maximum Power Tuning

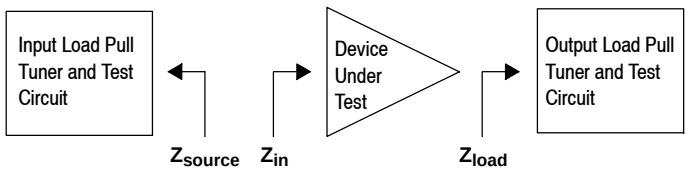
V_{DD} = 28 Vdc, I_{DQA} = 763 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.29 - j7.28	3.63 + j7.22	5.78 - j1.16	21.6	49.6	91	65.4	-22
2140	5.23 - j7.74	4.54 + j7.46	5.88 - j1.54	21.5	49.8	95	65.1	-21
2170	6.26 - j7.95	5.66 + j7.76	4.75 - j1.49	21.6	49.8	96	65.0	-23

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	4.29 - j7.28	3.84 + j7.59	6.49 - j2.11	19.4	50.6	114	65.3	-28
2140	5.23 - j7.74	4.91 + j8.02	6.10 - j1.54	19.5	50.4	110	65.9	-30
2170	6.26 - j7.95	6.28 + j8.14	5.82 - j2.06	19.4	50.7	117	65.7	-29

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning



V_{DD} = 28 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.76 - j5.24	2.87 + j5.85	2.36 - j4.99	14.4	54.7	292	54.6	-22
2140	3.54 - j5.55	3.73 + j6.27	2.61 - j5.09	14.6	54.7	292	55.0	-23
2170	5.02 - j5.82	5.01 + j6.41	2.80 - j5.30	14.6	54.6	288	53.5	-25

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.76 - j5.24	3.16 + j6.20	2.51 - j5.47	12.1	55.3	337	54.4	-28
2140	3.54 - j5.55	4.25 + j6.63	2.77 - j5.62	12.3	55.3	336	53.9	-29
2170	5.02 - j5.82	5.80 + j6.63	3.08 - j5.67	12.4	55.2	332	54.1	-31

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Peaking Side Load Pull Performance — Maximum Power Tuning

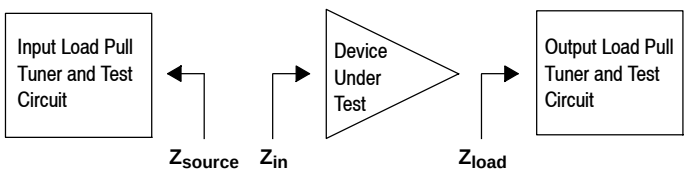
V_{DD} = 28 Vdc, V_{GSB} = 0.7 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.76 - j5.24	2.36 + j6.00	3.43 - j2.05	15.8	52.8	189	66.0	-29
2140	3.54 - j5.55	3.08 + j6.45	3.22 - j2.11	15.9	52.8	191	65.9	-31
2170	5.02 - j5.82	4.19 + j6.80	3.07 - j2.13	15.9	52.8	190	65.0	-33

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.76 - j5.24	2.74 + j6.36	3.71 - j2.53	13.7	53.7	233	65.3	-36
2140	3.54 - j5.55	3.67 + j6.84	3.57 - j2.44	13.8	53.6	231	65.1	-39
2170	5.02 - j5.82	5.15 + j7.06	3.45 - j2.52	13.8	53.7	234	64.3	-41

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

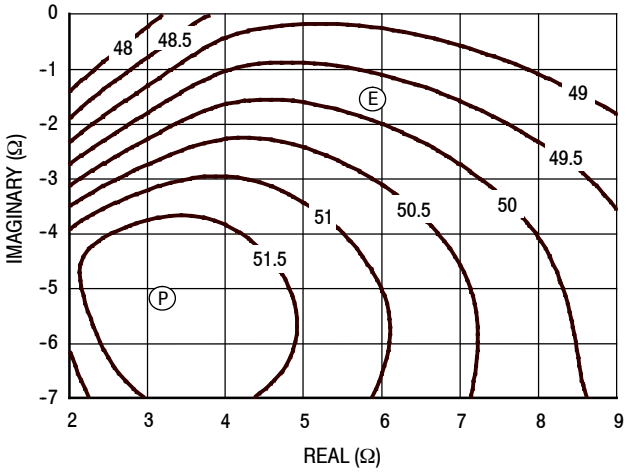


Figure 12. P1dB Load Pull Output Power Contours (dBm)

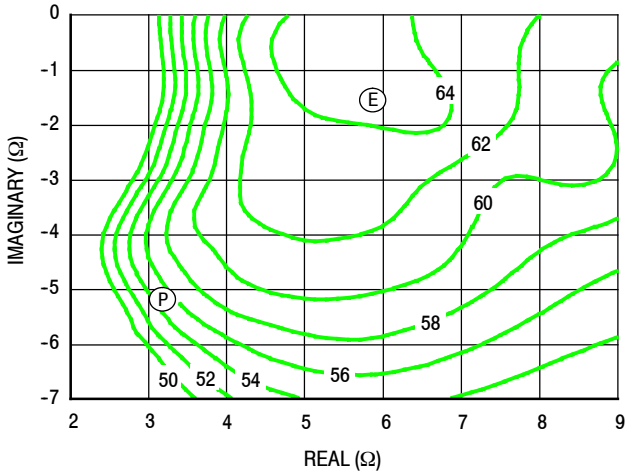


Figure 13. P1dB Load Pull Efficiency Contours (%)

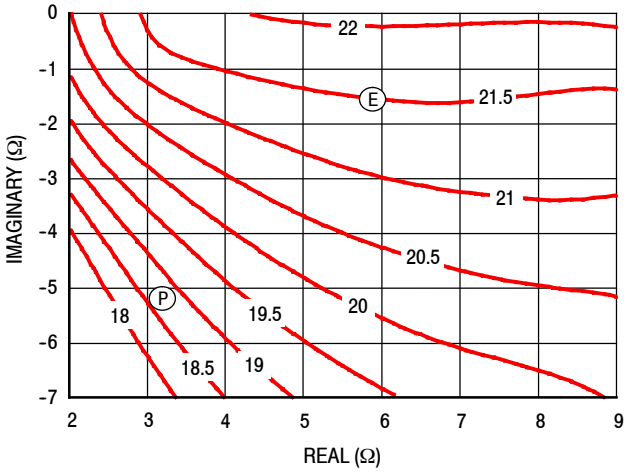


Figure 14. P1dB Load Pull Gain Contours (dB)

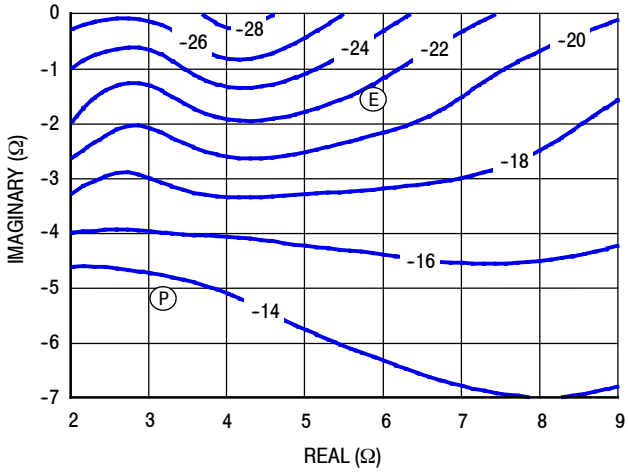


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

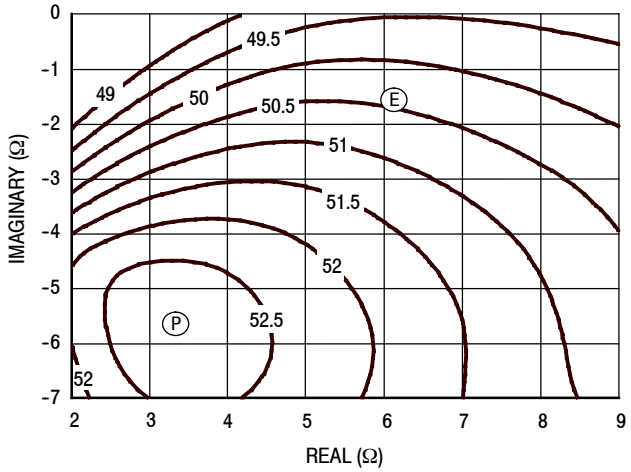


Figure 16. P3dB Load Pull Output Power Contours (dBm)

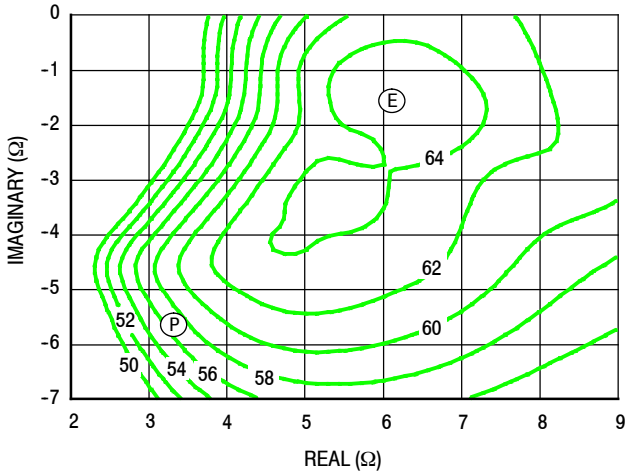


Figure 17. P3dB Load Pull Efficiency Contours (%)

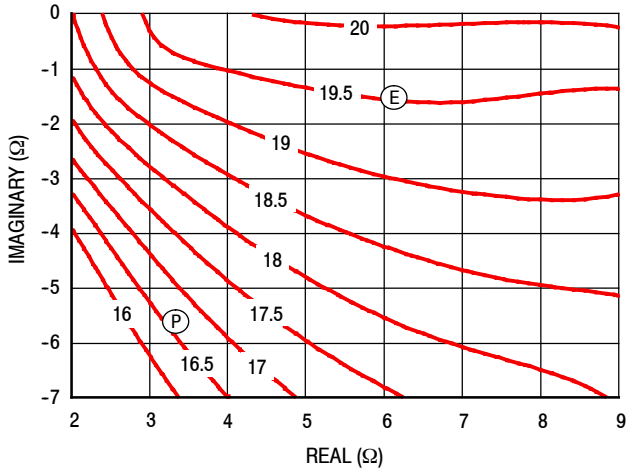


Figure 18. P3dB Load Pull Gain Contours (dB)

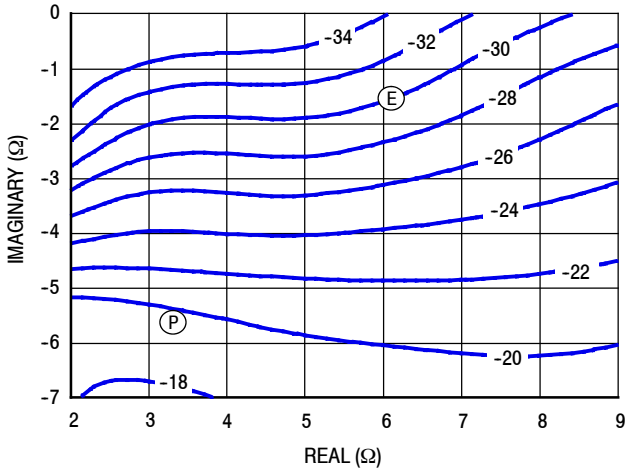


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

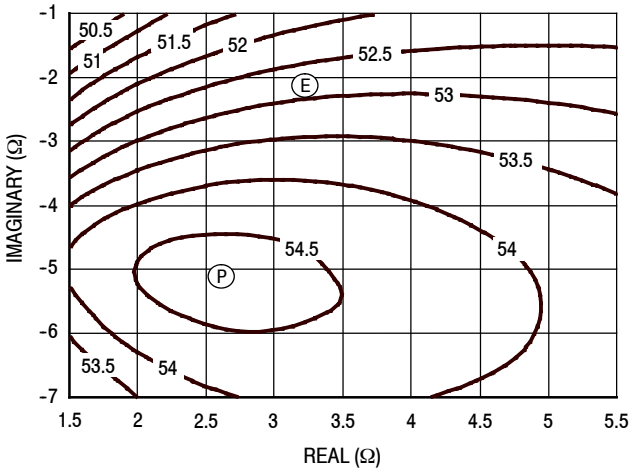


Figure 20. P1dB Load Pull Output Power Contours (dBm)

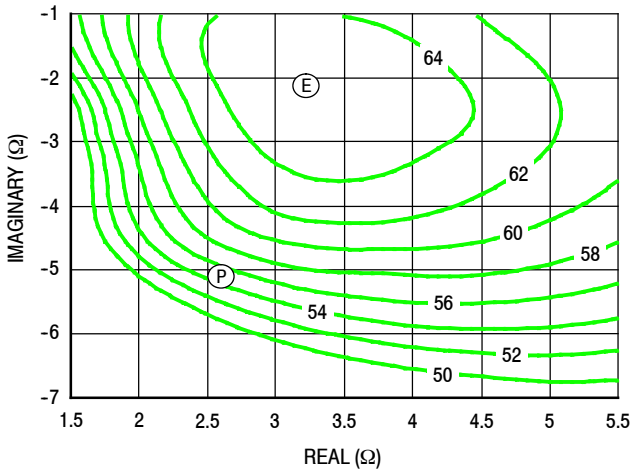


Figure 21. P1dB Load Pull Efficiency Contours (%)

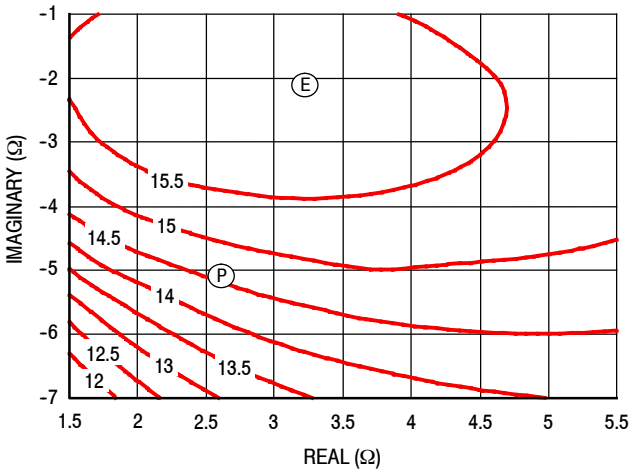


Figure 22. P1dB Load Pull Gain Contours (dB)

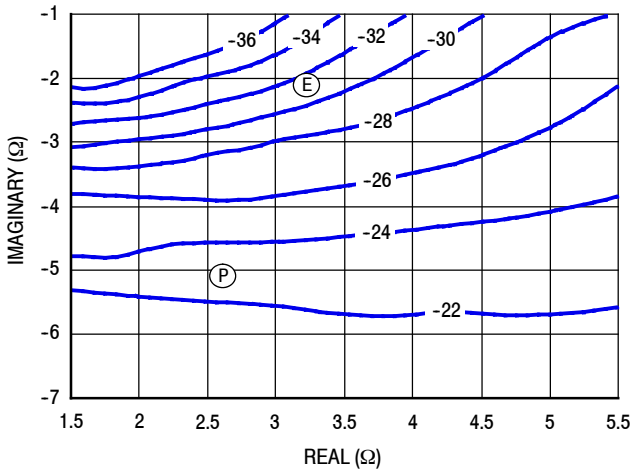


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

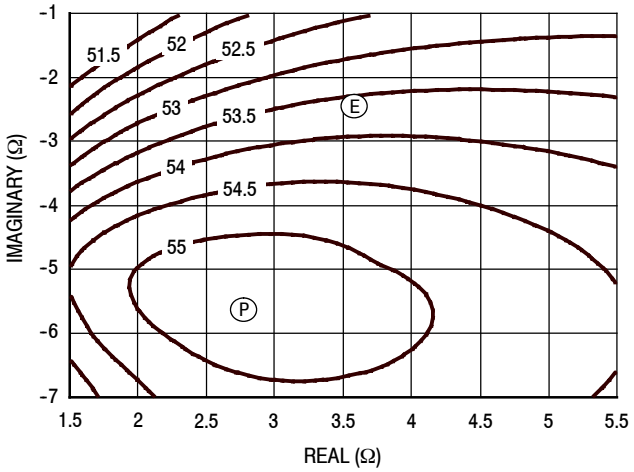


Figure 24. P3dB Load Pull Output Power Contours (dBm)

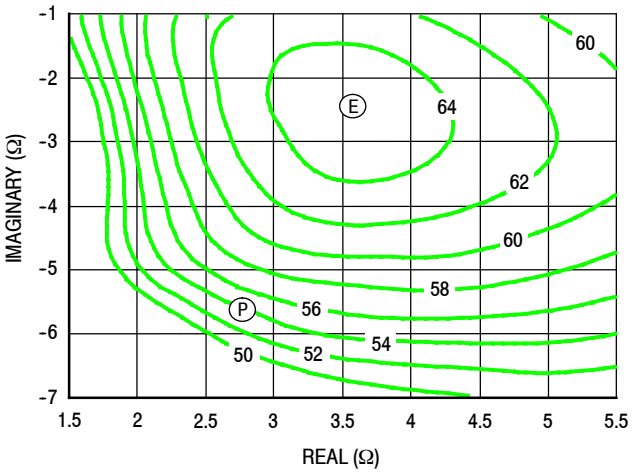


Figure 25. P3dB Load Pull Efficiency Contours (%)

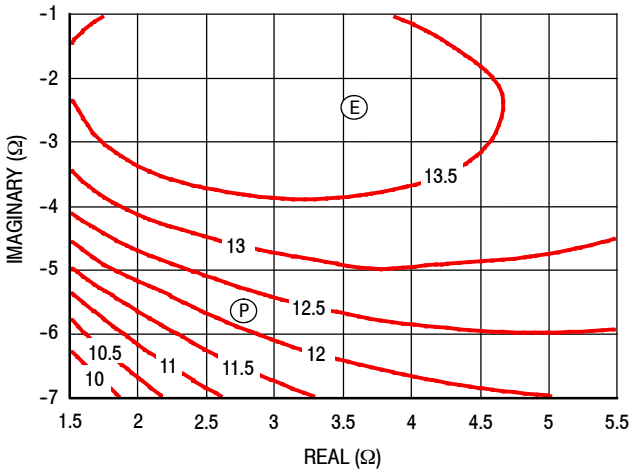


Figure 26. P3dB Load Pull Gain Contours (dB)

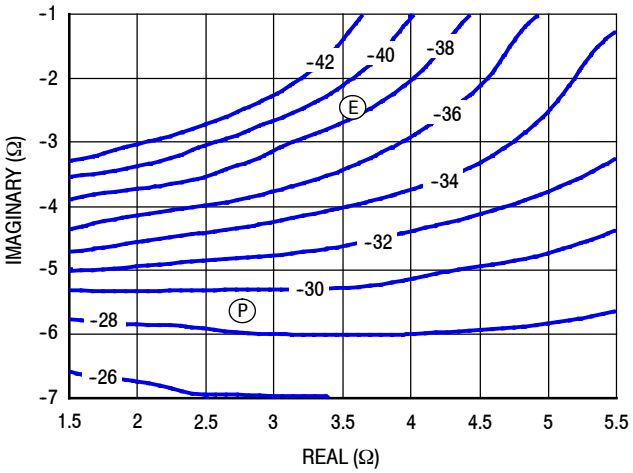


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

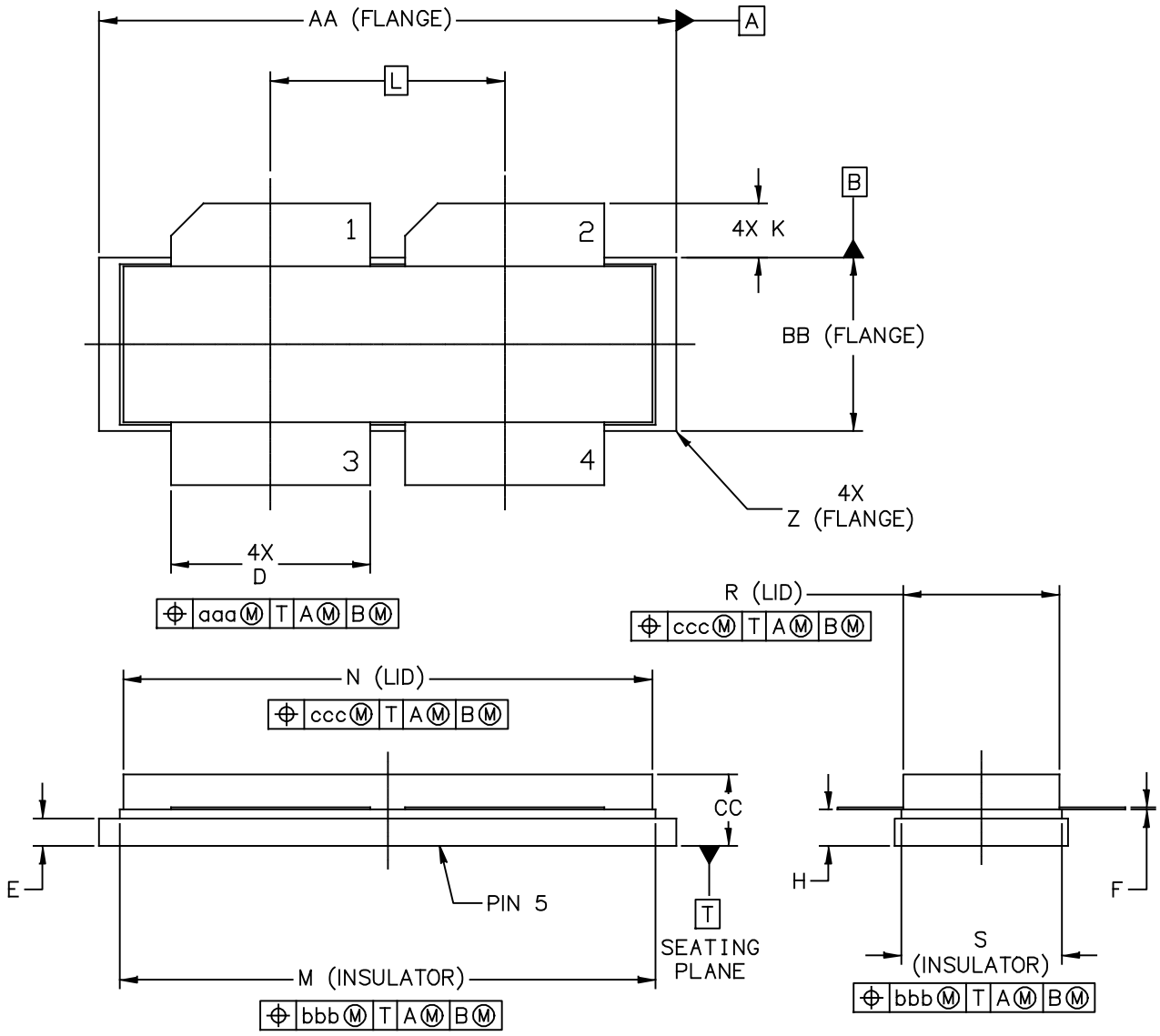
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-1230-4S	DOCUMENT NO: 98ARB18247C	REV: G
	STANDARD: NON-JEDEC	
	01 MAR 2013	

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM PACKAGE BODY

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
BB	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	Z	R.000	R.040	R0.00	R1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.10	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

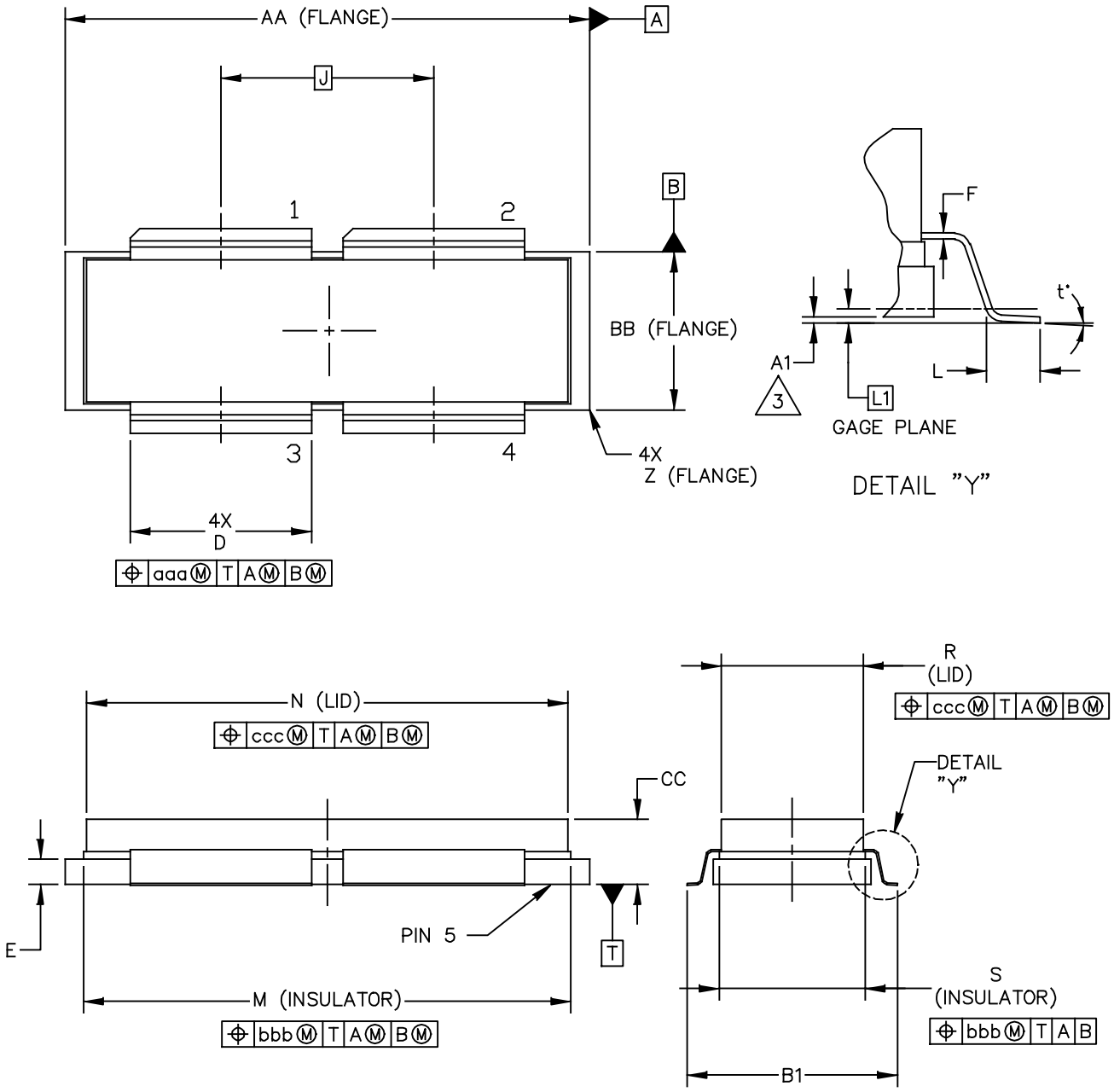
MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: NI–1230–4S

DOCUMENT NO: 98ARB18247C REV: G

STANDARD: NON–JEDEC

01 MAR 2013



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-1230-4S GULL	DOCUMENT NO: 98ASA00459D	REV: A
	STANDARD: NON-JEDEC	
	07 MAR 2013	

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
A1	–.001	.011	–0.03	0.28	S	.365	.375	9.27	9.53
BB	.395	.405	10.03	10.29	Z	R.000	R.040	R0.00	R1.02
B1	.564	.574	14.32	14.58	t°	0°	8°	0°	8°
CC	.170	.190	4.32	4.83					
D	.455	.465	11.56	11.81	aaa	.013		0.33	
E	.062	.066	1.57	1.68	bbb	.010		0.25	
F	.004	.007	0.10	0.18	ccc	.020		0.51	
J	.540 BSC		13.72 BSC						
L	.038	.046	0.97	1.17					
L1	.01 BSC		0.25 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: NI–1230–4S GULL

DOCUMENT NO: 98ASA00459D REV: A

STANDARD: NON–JEDEC

07 MAR 2013

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2013	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AFT21H350W03S
Rev. 0, 9/2013