



Kinetis K22F 512KB Flash 80-Pin WLCSP

120 MHz Cortex-M4 Based Microcontroller with FPU

The K22 product family members are optimized for space-constrained, cost-sensitive applications requiring lowpower, USB connectivity, and processing efficiency with a floating point unit. These devices share the comprehensive enablement and scalability of the Kinetis family.

This product offers:

- Run power consumption down to 156 μ A/MHz and static power consumption down to 3.8 μ A, full state retention and 6 μ S wakeup. Lowest static mode down to 140 nA.
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO voltage regulator. USB FS device crystal-less functionality.

MK22FN512CAP12R
MK22FN256CAP12R
MK22FN512CBP12R



80 WLCSP (AP) 80 WLCSP (BP)
4.13 x 3.56 x 0.564 mm 4.13 x 3.56 x 0.321 mm
Pitch 0.4 mm Pitch 0.4 mm

Performance

- 120 MHz ARM® Cortex®-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

Memories and memory interfaces

- 512 or 256 KB of embedded flash, and 128 KB of RAM
- FlexBus external bus interface
- Serial programming interface (EzPort)
- Preprogrammed Kinetis flashloader for one-time, in-system factory programming

System peripherals

- Flexible low-power modes, multiple wake up sources
- 16-channel DMA controller
- Independent external and software watchdog monitor

Clocks

- Two crystal oscillators: 32 kHz (RTC) and 32-40 kHz or 3-32 MHz
- Three internal oscillators: 32 kHz, 4 MHz, and 48 MHz
- Multi-purpose clock generator with PLL and FLL

Security and integrity modules

- Hardware CRC module
- 128-bit unique identification (ID) number per chip
- Hardware random-number generator
- Flash access control to protect proprietary software

Human-machine interface

- 52 general-purpose I/O (GPIO)

Analog modules

- Two 16-bit SAR ADCs (1.2 MS/s in 12bit mode)
- Up to two 12-bit DACs
- Two analog comparators (CMP) with 6-bit DAC
- Accurate internal voltage reference

Communication interfaces

- USB LS/FS OTG 2.0 with on-chip transceiver and USB LDO voltage regulator
- USB full-speed device crystal-less operation
- Two SPI modules
- Three UART modules and one low-power UART
- Two I2C: Support for up to 1 Mbps operation
- I2S module

Timers

- Two 8-ch general-purpose/PWM timers
- Two 2-ch general-purpose timers with quadrature decoder functionality
- Periodic interrupt timers
- 16-bit low-power timer
- Real-time clock with independent power domain
- Programmable delay block

Operating Characteristics

- Voltage range (including flash writes): 1.71 to 3.6 V
- Temperature range (ambient): -40 to 85°C

Ordering Information

Part Number	Memory		Maximum number of I/Os
	Flash (KB)	SRAM (KB)	
MK22FN512CAP12R	512	128	52
MK22FN256CAP12R	256	128	52
MK22FN512CBP12R	512	128	52

Related Resources

Type	Description	Document
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector	KINETISKMCUSELGD
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K22P121M120SF7RM
Data Sheet	The Data Sheet is this document. It includes electrical characteristics and signal connections.	K22P80M120SF7
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_xN50M ¹
Package drawing	Package dimensions are provided by part number: <ul style="list-style-type: none"> • MK22FN512CAP12R • MK22FN256CAP12R • MK22FN512CBP12R 	Package drawing: <ul style="list-style-type: none"> • 98ASA00710D • 98ASA00710D • 98ASA00820D

1. To find the associated resource, go to [freescale.com](#) and perform a search using this term with the x replaced by the revision of the device you are using.

[Figure 1](#) shows the functional modules in the chip.

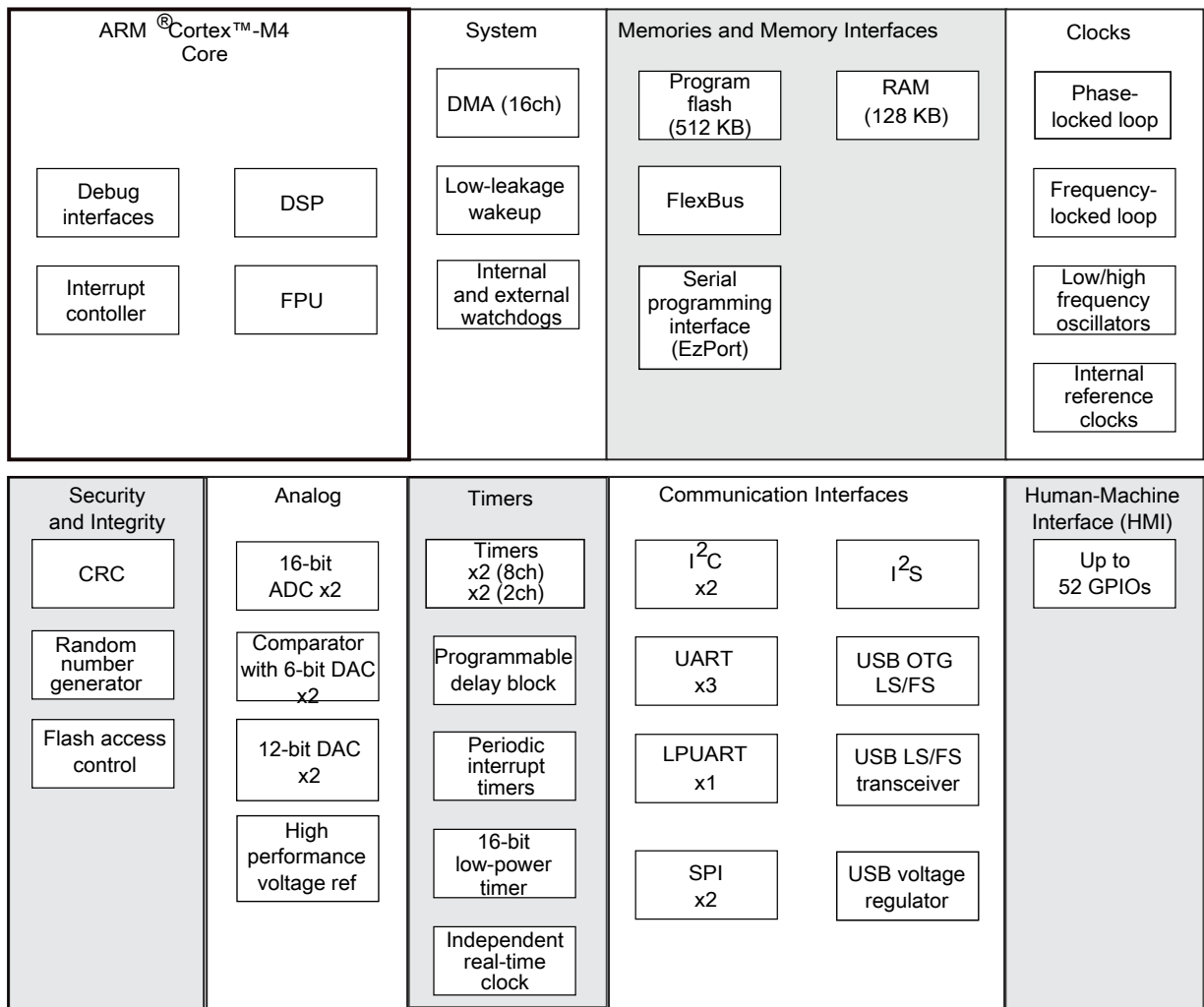


Figure 1. Functional block diagram

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1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	1	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

General

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	169	mA
V_{DIO}	Digital input voltage	-0.3	$V_{DD} + 0.3$	V
V_{AIO}	Analog ¹	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	
V _{DD} – V _{DDA}	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
V _{SS} – V _{SSA}	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{BAT}	RTC battery supply voltage	1.71	3.6	V	
V _{IH}	Input high voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V 	0.7 × V _{DD}	—	V	
		0.75 × V _{DD}	—	V	
V _{IL}	Input low voltage <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V 	—	0.35 × V _{DD}	V	
		—	0.3 × V _{DD}	V	
V _{HYS}	Input hysteresis	0.06 × V _{DD}	—	V	
I _{ICIO}	Analog and I/O pin DC injection current — single pin <ul style="list-style-type: none"> • V_{IN} < V_{SS}-0.3V (Negative current injection) 	-3	—	mA	1
I _{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection 	-25	—	mA	
V _{ODPU}	Open drain pullup voltage level	V _{DD}	V _{DD}	V	2
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	—	V	
V _{RFVBAT}	V _{BAT} voltage required to retain the VBAT register file	V _{POR_VBAT}	—	V	

1. All analog and I/O pins are internally clamped to V_{SS} through ESD protection diodes. If V_{IN} is less than V_{IO_MIN} or greater than V_{IO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN}) / |I_{ICIO}|$.
2. Open drain outputs must be pulled to V_{DD}.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling V _{DD} POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V _{LVW1H}	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> • Level 1 falling (LVWV=00) 	2.62	2.70	2.78	V	1

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V _{LVW1L}	Low-voltage warning thresholds — low range • Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	1
V _{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V _{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{OH}	Output high voltage — Normal drive pad except RESET_B 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -5 mA 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -2.5 mA	V _{DD} - 0.5 V _{DD} - 0.5	— —	— —	V V	1
V _{OH}	Output high voltage — High drive pad except RESET_B 2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OH} = -20 mA 1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OH} = -10 mA	V _{DD} - 0.5 V _{DD} - 0.5	— —	— —	V V	1
I _{OHT}	Output high current total for all ports	—	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{OL}	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA	—	—	0.5	V	1
V _{OL}	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 20 mA	—	—	0.5	V	1
V _{OL}	Output low voltage — RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 3 mA	—	—	0.5	V	
V _{OL}	Output low voltage — RESET_B					
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 10 mA	—	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	μA	1, 2
I _{IN}	Input leakage current (per pin) for full temperature range					
	High drive port pins	—	0.004	0.5	μA	
I _{IN}	Input leakage current (total all pins) for full temperature range	—	—	1.0	μA	2
R _{PU}	Internal pullup resistors	20	—	50	kΩ	3
R _{PD}	Internal pulldown resistors	20	—	50	kΩ	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V_{DD}=3.6V
3. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}
4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 80 MHz
- Bus clock = 40 MHz
- FlexBus clock = 20 MHz
- Flash clock = 20 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V _{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	• VLLS0 → RUN	—	—	140	μs	
	• VLLS1 → RUN	—	—	140	μs	
	• VLLS2 → RUN	—	—	80	μs	
	• VLLS3 → RUN	—	—	80	μs	
	• LLS2 → RUN	—	—	6	μs	
	• LLS3 → RUN	—	—	6	μs	
	• VLPS → RUN	—	—	5.7	μs	
	• STOP → RUN	—	—	5.7	μs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash					

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 1.8V @ 3.0V	— —	28.0 28.0	29.33 29.33	mA mA	2, 3, 4
I _{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	— —	25.6 25.7	26.93 27.03	mA mA	2
I _{DD_HSRUN}	High Speed Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V	— —	35.5 35.6	36.83 36.93	mA mA	5
I _{DD_RUN}	Run mode current in Compute operation — CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	— —	17.5 17.5	18.83 18.83	mA mA	3, 4, 6
I _{DD_RUN}	Run mode current in Compute operation — code executing from flash @ 1.8V @ 3.0V	— —	15.10 15.10	17.10 17.33	mA mA	6
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	— —	16.6 16.8	17.93 18.13	mA mA	7
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V • @ 25°C • @ 70°C • @ 85°C	— — — —	22.8 22.9 23.1 23.5	24.13 24.23 24.43 24.83	mA mA mA mA	8
I _{DD_RUN}	Run mode current — Compute operation, code executing from flash @ 1.8V @ 3.0V • @ 25°C • @ 70°C • @ 85°C	— — — —	15.1 15.1 15.4 15.6	16.43 16.43 16.73 16.93	mA mA mA mA	9
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	9.3	10.63	mA	7

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.4	6.73	mA	10
I _{DD_VLPR}	Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	— —	0.88 0.89	1.02 1.03	mA mA	3, 4, 11
I _{DD_VLPR}	Very-low-power run mode current in Compute operation, code executing from flash @ 1.8V @ 3.0V	— —	0.62 0.63	0.77 0.77	mA mA	11
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.76	0.90	mA	12
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.2	1.34	mA	13
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.45	0.59	mA	14
I _{DD_STOP}	Stop mode current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C	— — —	0.28 0.34 0.38	0.37 0.51 0.55	mA mA mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C	— — —	8.7 31.1 50.3	18.10 79.55 110.15	μA μA μA	
I _{DD_LLS3}	Low leakage stop mode 3 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C	— — —	3.8 12.5 20.2	5.65 28.75 47.60	μA μA μA	
I _{DD_LLS2}	Low leakage stop mode 2 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C	— — —	3.0 7.8 12.3	4.10 16.40 30.15	μA μA μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C	— — —	2.8 9.5 15.3	3.95 21.25 34.65	μA μA μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C	— — —	1.9 4.5 6.8	2.45 8.50 12.15	μA μA μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	@ -40°C to 25°C	—	0.73	1.42	μA	
	@ 70°C	—	1.8	3.90	μA	
	@ 85°C	—	3.0	5.25	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	—	0.43	0.55	μA	
	@ 70°C	—	1.4	2.45	μA	
	@ 85°C	—	2.6	4.00	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.14	0.24	μA	
	@ 70°C	—	1.1	2.15	μA	
	@ 85°C	—	2.3	3.85	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	@ -40°C to 25°C	—	0.18	0.21	μA	
	@ 70°C	—	0.66	0.86	μA	
	@ 85°C	—	1.52	2.24	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers					
	@ 1.8V					
	• @ -40°C to 25°C	—	0.59	0.70	μA	15
	• @ 70°C	—	1.00	1.3	μA	
	• @ 85°C	—	1.76	2.59	μA	
	@ 3.0V					
	• @ -40°C to 25°C	—	0.71	0.84	μA	
	• @ 70°C	—	1.22	1.59	μA	
	• @ 85°C	—	2.08	3.06	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. Cache on and prefetch on, low compiler optimization.
4. Coremark benchmark compiled using IAR 7.2 with optimization level low.
5. 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
6. 80 MHz core and system clock, 40 MHz bus clock, and 26.67 MHz flash clock. MCG configured for PEE mode. Compute operation.
7. 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.

General

8. 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
9. 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. Compute operation.
10. 25MHz core and system clock, 25MHz bus clock, and 25MHz FlexBus and flash clock. MCG configured for FEI mode.
11. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
12. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
13. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
14. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
15. Includes 32kHz oscillator current and RTC operation.

Table 7. Low power mode peripheral adders—typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{IREFSTEN4MHz}	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I _{IREFSTEN32KHz}	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I _{EREFSTEN4MHz}	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
I _{EREFSTEN32KHz}	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I _{48MIRC}	48 Mhz internal reference clock	350	350	350	350	350	350	μA
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA

Table continues on the next page...

Table 7. Low power mode peripheral adders—typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V _{DD} and V _{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz. MCG in PEE mode at frequencies greater than 100 MHz.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

General

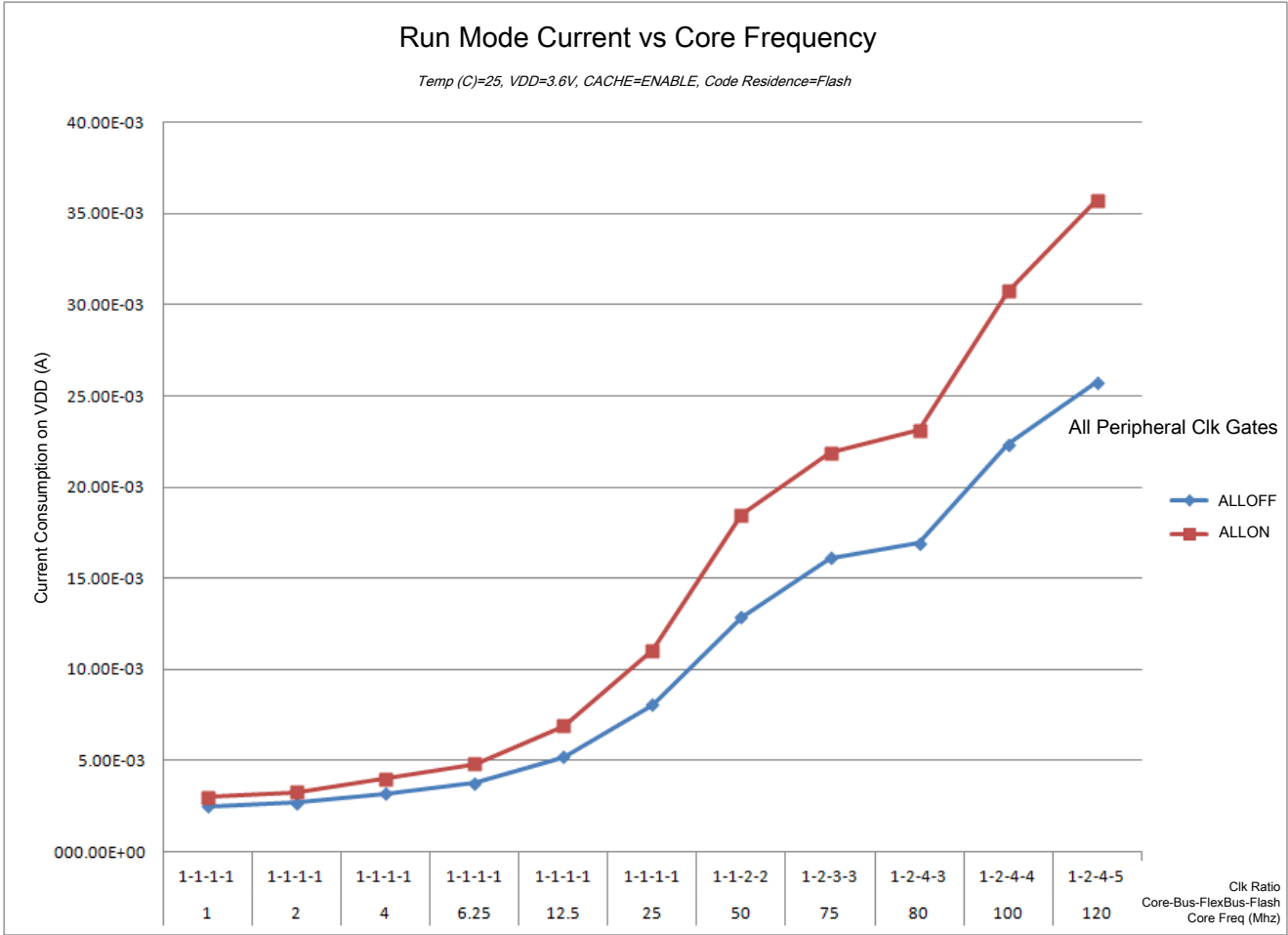


Figure 3. Run mode supply current vs. core frequency

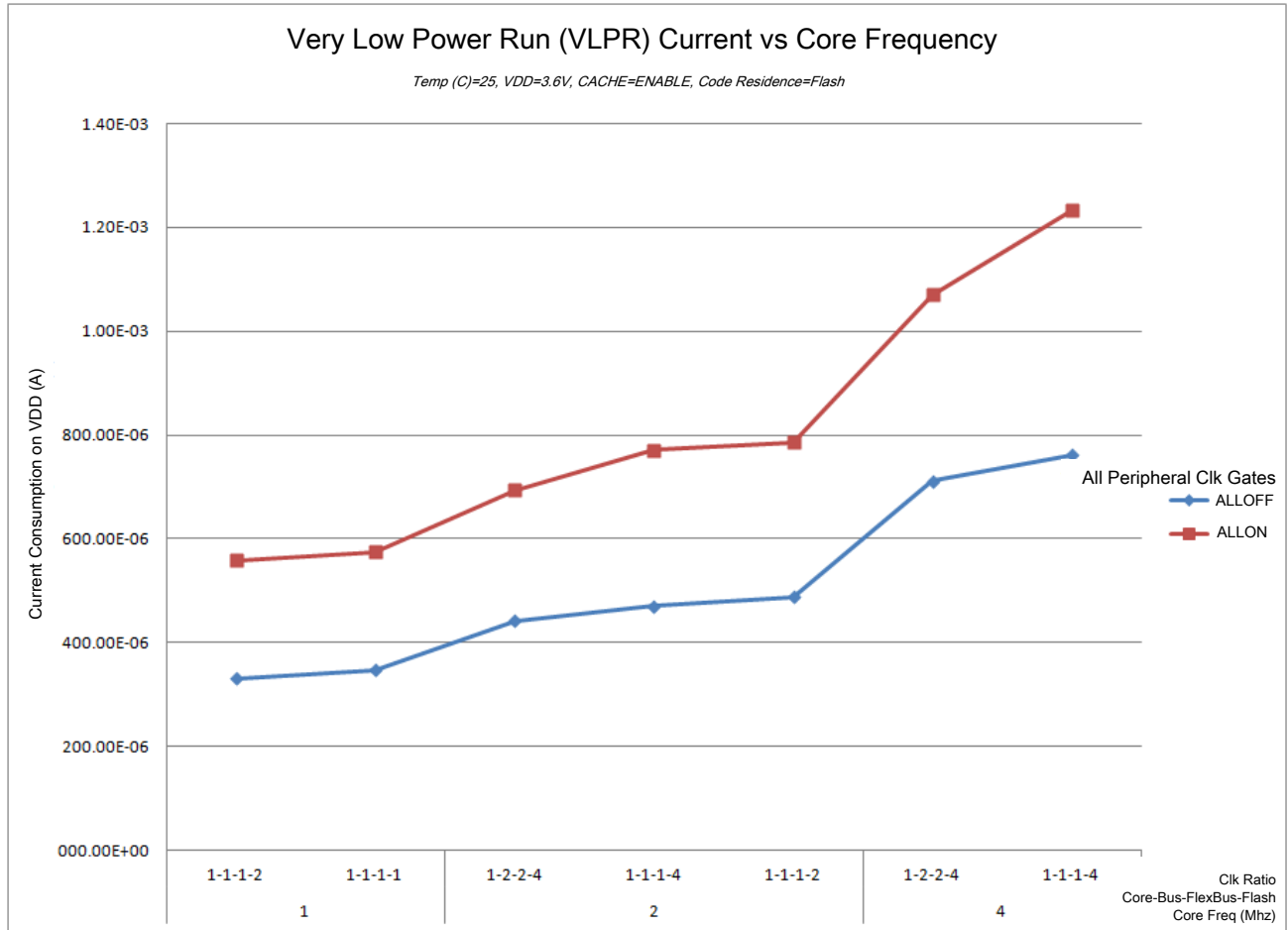


Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors for 64 LQFP package

Parameter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V _{EME}	Device configuration, test conditions and EM testing per standard IEC 61967-2. Supply voltages: <ul style="list-style-type: none"> VREGIN (USB) = 5.0 V VDD = 3.3 V Temp = 25°C	FSYS = 120 MHz FBUS = 60 MHz External crystal = 8 MHz	150 kHz–50 MHz	14	dBuV	1, 2, 3
			50 MHz–150 MHz	23		
			150 MHz–500 MHz	23		
			500 MHz–1000 MHz	9		
			IEC level	L		4

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MK22FN512VLH12 .

General

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV .

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f _{SYS}	System and core clock	—	120	MHz	
f _{BUS}	Bus clock	—	60	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f _{SYS}	System and core clock	—	80	MHz	
f _{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f _{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	30	MHz	
f _{FLASH}	Flash clock	—	26.67	MHz	
f _{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					

Table continues on the next page...

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f _{SYS}	System and core clock	—	4	MHz	
f _{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f _{FLASH}	Flash clock	—	1	MHz	
f _{ERCLK}	External reference clock	—	16	MHz	
f _{LPTMR_pin}	LPTMR clock	—	25	MHz	
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f _{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	Mode select ($\overline{\text{EZP_CS}}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time <ul style="list-style-type: none"> • Slew disabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled <ul style="list-style-type: none"> • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ 	— — — —	10 5 30 16	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.

General

2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _J	Die junction temperature	-40	95	°C	
T _A	Ambient temperature	-40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

2.4.2 Thermal attributes

Board type	Symbol	Description	80 WLCSP (AP)	80 WLCSP (BP)	Unit	Notes
Single-layer (1s)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	49.0	102.4	°C/W	1
Four-layer (2s2p)	R _{θJA}	Thermal resistance, junction to ambient (natural convection)	36.6	47.3	°C/W	2
Single-layer (1s)	R _{θJMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	39.3	86.4	°C/W	3
Four-layer (2s2p)	R _{θJMA}	Thermal resistance, junction to ambient (200	32.1	42.7	°C/W	3

Table continues on the next page...

Board type	Symbol	Description	80 WLCSP (AP)	80 WLCSP (BP)	Unit	Notes
		ft./min. air speed)				
—	$R_{\theta JB}$	Thermal resistance, junction to board	36.8	25.7	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	0.2	4.2	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.1	0.2	°C/W	6

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 13. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation <ul style="list-style-type: none"> • Serial wire debug 	0	33	MHz
S2	SWD_CLK cycle period	1/S1	—	ns

Table continues on the next page...

Table 13. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
S3	SWD_CLK clock pulse width • Serial wire debug	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

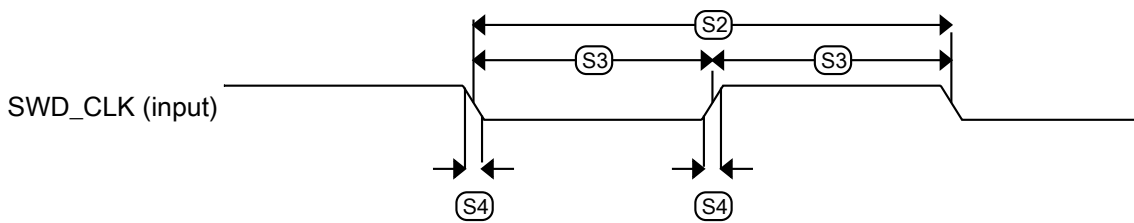


Figure 5. Serial wire clock input timing

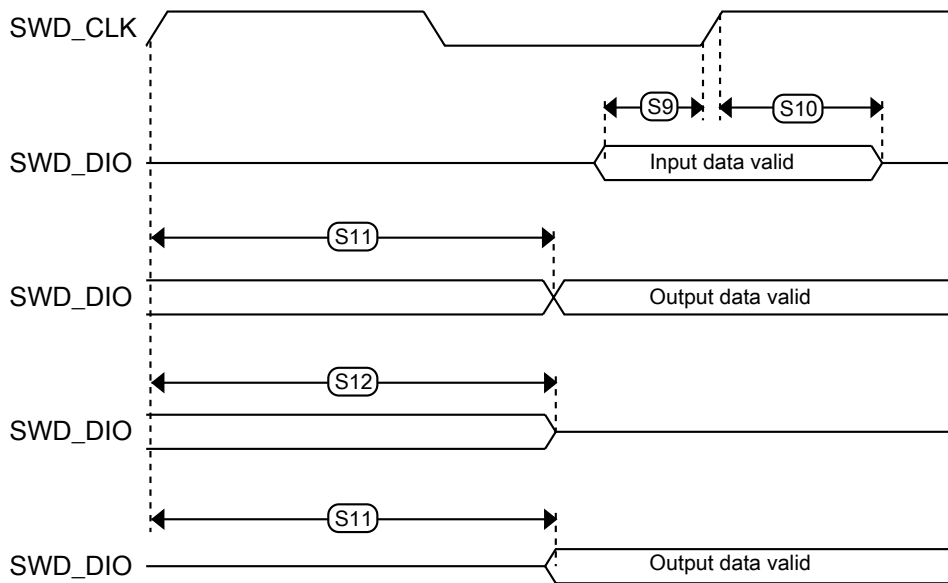


Figure 6. Serial wire data timing

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG 	0 0	10 20	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG 	50 25	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 15. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG 	0 0	10 15	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> • Boundary Scan • JTAG and CJTAG 	50 33	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns

Table continues on the next page...

Table 15. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns



Figure 7. Test clock input timing

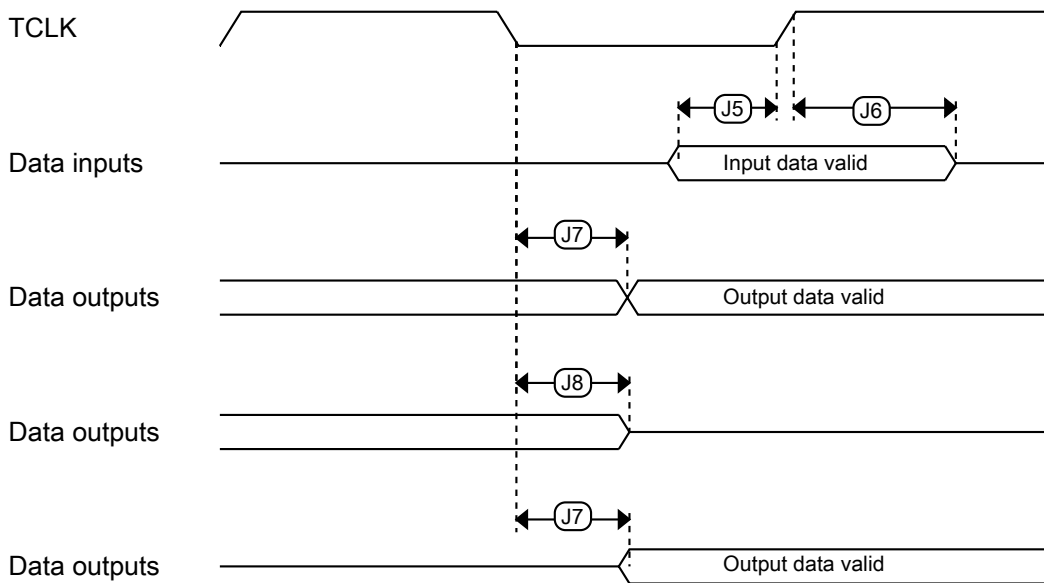


Figure 8. Boundary scan (JTAG) timing



Figure 9. Test Access Port timing

Figure 10. $\overline{\text{TRST}}$ timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 16. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz		
$\Delta f_{\text{ints_t}}$	Total deviation of internal reference frequency (slow clock) over voltage and temperature	—	+0.5/-0.7	± 2	%		
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% f_{dco}	1	
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 2	% f_{dco}	1, 2	
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1.5	% f_{dco}	1	
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz		
$\Delta f_{\text{intf_ft}}$	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C	—	+1/-2	± 5	% $f_{\text{intf_ft}}$		
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz		
$f_{\text{loc_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints_t}}$	—	—	kHz		
$f_{\text{loc_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints_t}}$	—	—	kHz		
FLL							
$f_{\text{fll_ref}}$	FLL reference frequency range	31.25	—	39.0625	kHz		
f_{dco}	DCO output frequency range	Low range (DRS=00) $640 \times f_{\text{fll_ref}}$	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) $1280 \times f_{\text{fll_ref}}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{\text{fll_ref}}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{\text{fll_ref}}$	80	83.89	100	MHz	
$f_{\text{dco_t_DMX3}}_2$	DCO output frequency	Low range (DRS=00) $732 \times f_{\text{fll_ref}}$	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) $1464 \times f_{\text{fll_ref}}$	—	47.97	—	MHz	
		Mid-high range (DRS=10)	—	71.99	—	MHz	

Table continues on the next page...

Table 16. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter <ul style="list-style-type: none"> $f_{VCO} = 48$ MHz $f_{VCO} = 98$ MHz 	—	—	—	ps	
$t_{fil_acquire}$	FLL target frequency acquisition time	—	—	1	ms	7
PLL						
f_{vco}	VCO operating frequency	48.0	—	120	MHz	
I_{pll}	PLL operating current <ul style="list-style-type: none"> PLL @ 96 MHz ($f_{osc_hi_1} = 8$ MHz, $f_{pll_ref} = 2$ MHz, VDIV multiplier = 48) 	—	1060	—	μ A	8
I_{pll}	PLL operating current <ul style="list-style-type: none"> PLL @ 48 MHz ($f_{osc_hi_1} = 8$ MHz, $f_{pll_ref} = 2$ MHz, VDIV multiplier = 24) 	—	600	—	μ A	8
f_{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) <ul style="list-style-type: none"> $f_{vco} = 48$ MHz $f_{vco} = 100$ MHz 	—	120	—	ps	9
		—	75	—	ps	
J_{acc_pll}	PLL accumulated jitter over 1 μ s (RMS) <ul style="list-style-type: none"> $f_{vco} = 48$ MHz $f_{vco} = 100$ MHz 	—	1350	—	ps	9
		—	600	—	ps	
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	10

- This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2.0 V \leq VDD \leq 3.6 V.
- These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
- The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
- These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
- The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- Excludes any oscillator currents that are also consuming power while PLL is in operation.
- This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 IRC48M specifications

Table 17. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	μ A	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0°C to 70°C Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.2	± 0.5	$\%f_{irc48m}$	1
$\Delta f_{irc48m_ol_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.4	± 1	$\%f_{irc48m}$	1
$\Delta f_{irc48m_ol_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.4 ± 0.5	± 1 ± 1.5	$\%f_{irc48m}$	1
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	2
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	μ s	3

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean \pm 3 sigma).
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
 - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1 or
 - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10 or MCG_C5[PLLCLKEN0]=1, or
 - SIM_SOPT2[PLLFLLSEL]=11

3.3.3 Oscillator electrical specifications

3.3.3.1 Oscillator DC electrical specifications

Table 18. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz 	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I _{DDOSC}	Supply current — high-gain mode (HGO=1) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz 	—	25	—	μA	1
		—	400	—	μA	
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	

Table continues on the next page...

Table 18. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V _{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.3.3.2 Oscillator frequency specifications

Table 19. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

- Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.3.4 32 kHz oscillator electrical characteristics

3.3.4.1 32 kHz oscillator DC electrical specifications

Table 20. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	$M\Omega$
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}^1	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.4.2 32 kHz oscillator frequency specifications

Table 21. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

- Proper PC board layout procedures must be followed to achieve specifications.
- This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
- The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 22. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	—
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versblk}256\text{k}}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 23. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{blk}256\text{k}}$	Read 1s Block execution time • 256 KB program flash	—	—	1.7	ms	1
$t_{rd1\text{sec}2\text{k}}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
$t_{pgm\text{chk}}$	Program Check execution time	—	—	45	μs	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	—
$t_{ers\text{blk}256\text{k}}$	Erase Flash Block execution time • 256 KB program flash	—	250	1500	ms	2
$t_{ers\text{scr}}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	—	1.8	ms	1
$t_{rd\text{once}}$	Read Once execution time	—	—	30	μs	1
$t_{pgm\text{once}}$	Program Once execution time	—	100	—	μs	—
$t_{ers\text{all}}$	Erase All Blocks execution time	—	500	3000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 24. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA

Table continues on the next page...

Table 24. Flash high voltage current behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	—
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years	—
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.4.2 EzPort switching specifications

Table 26. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{sys} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	f _{sys} /8	MHz
EP2	$\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion	2 x t _{EZP_CK}	—	ns
EP3	$\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	25	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state	—	12	ns

Peripheral operating requirements and behaviors

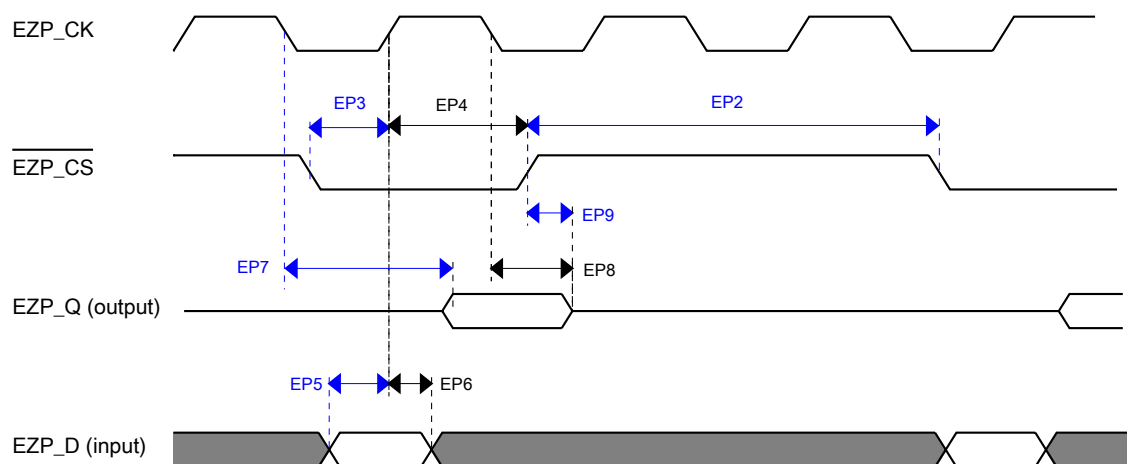


Figure 11. EzPort Timing Diagram

3.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 27. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	15	ns	
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	14.5	—	ns	
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSI[1:0], FB_ALE, and FB_TS.

2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 28. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	21.5	ns	
FB3	Address, data, and control output hold	-1.0	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	20.0	—	ns	
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, $\overline{\text{FB_R/W}}$, $\overline{\text{FB_TBST}}$, $\overline{\text{FB_TSIZ}}[1:0]$, $\overline{\text{FB_ALE}}$, and $\overline{\text{FB_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Peripheral operating requirements and behaviors

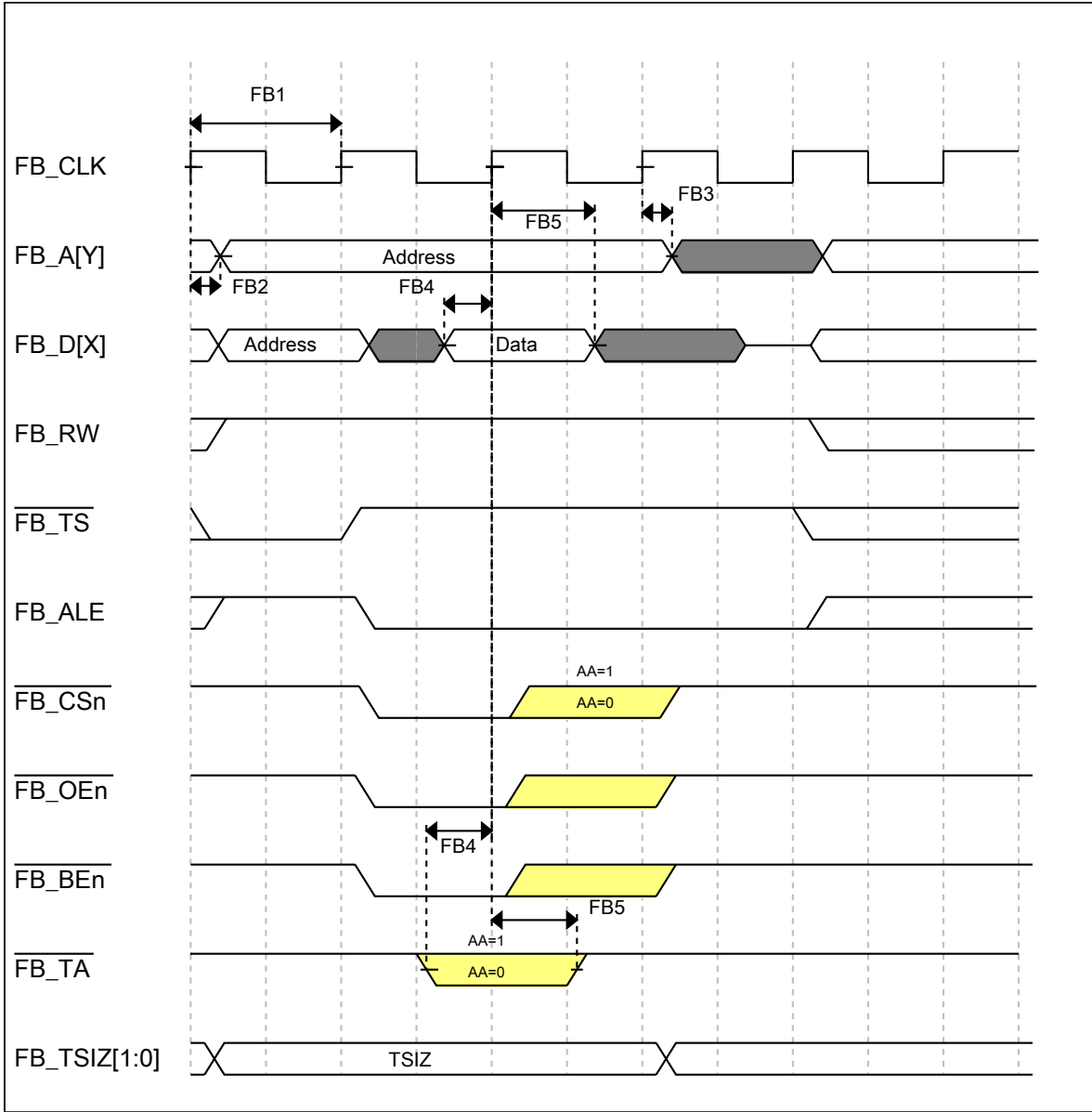


Figure 12. FlexBus read timing diagram

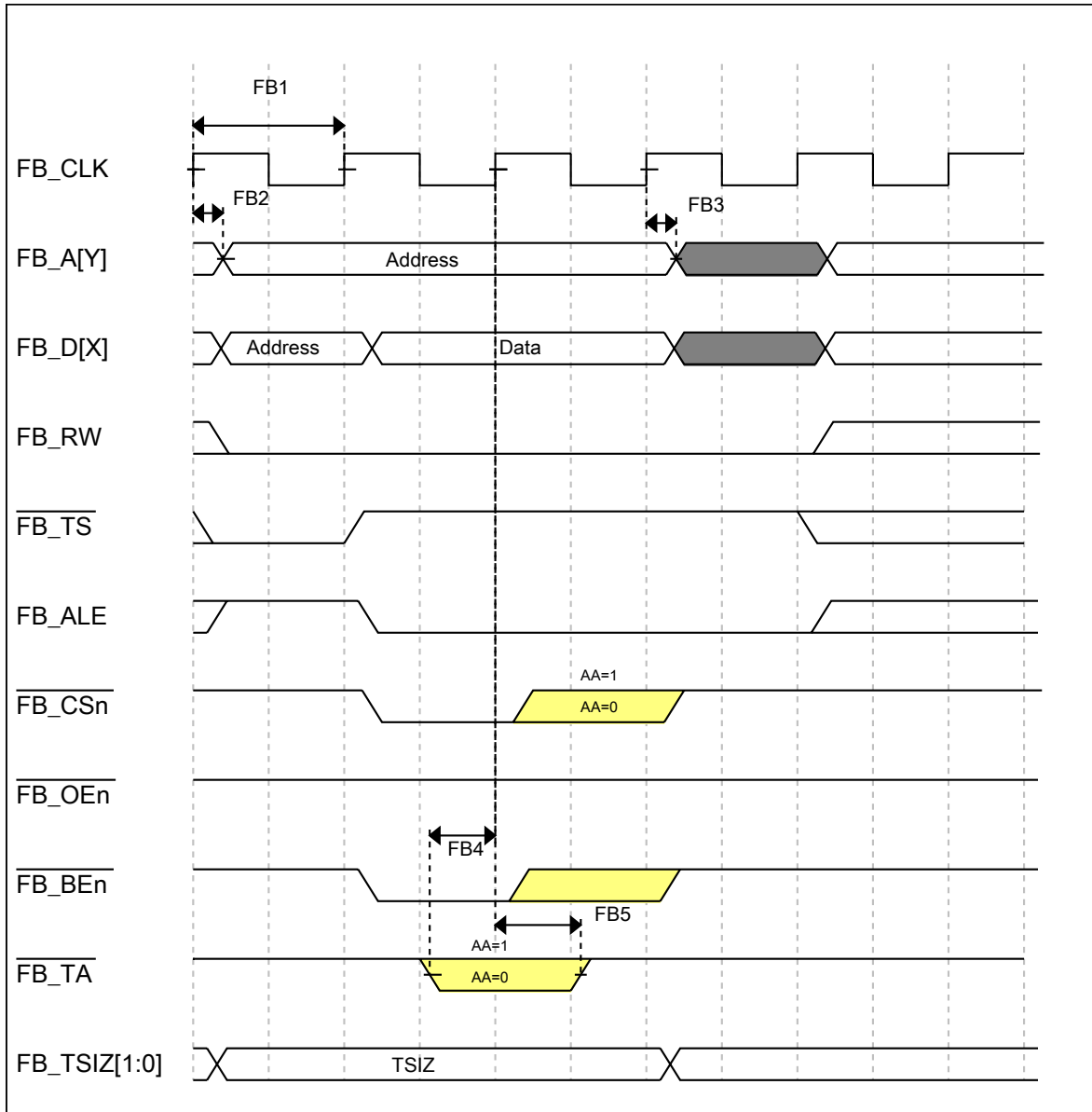


Figure 13. FlexBus write timing diagram

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 29](#) and [Table 30](#) are achievable on the differential pins ADCx_DPx, ADCx_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

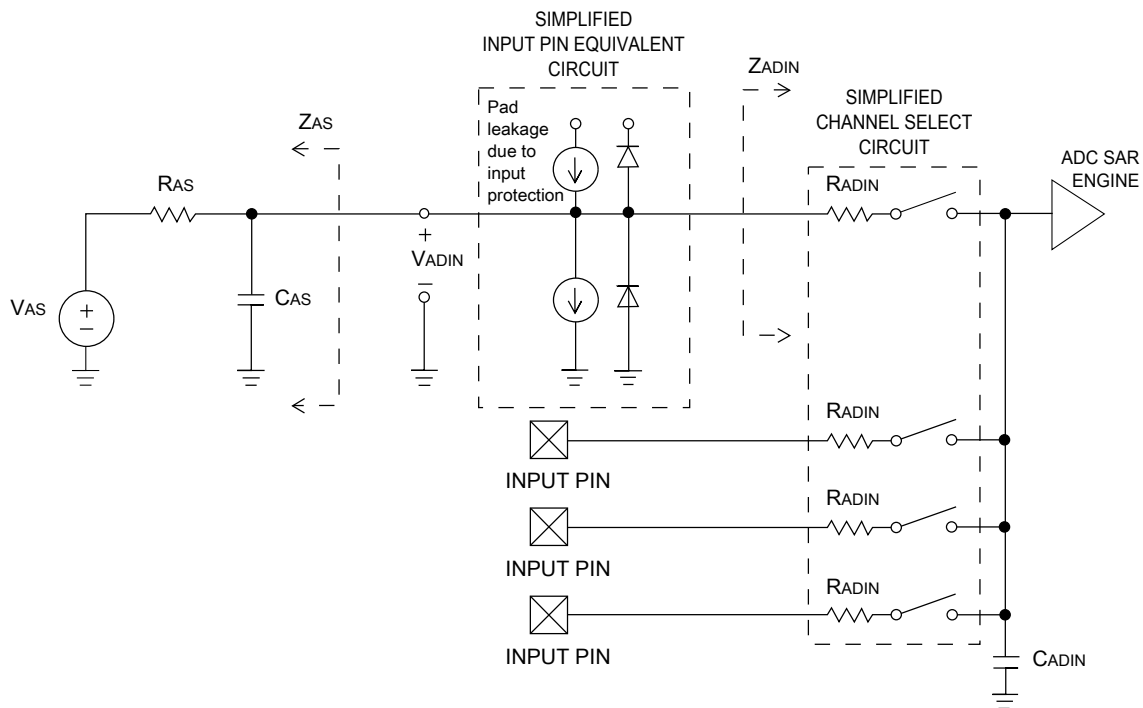
Table 29. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} – V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} – V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	<ul style="list-style-type: none"> 16-bit differential mode All other modes 	V _{REFL} V _{REFL}	— —	31/32 * V _{REFH} V _{REFH}	V	
C _{ADIN}	Input capacitance	<ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes 	— —	8 4	10 5	pF	
R _{ADIN}	Input series resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance (external)	13-bit / 12-bit modes f _{ADCK} < 4 MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C _{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	5
C _{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging	37	—	461	Ksps	5

Table 29. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
		Continuous conversions enabled, subsequent conversion time					

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8\ \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to $< 1\text{ ns}$.
4. To use the maximum ADC conversion clock frequency, $\text{CFG2}[\text{ADHSC}]$ must be set and $\text{CFG1}[\text{ADLPC}]$ must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

**Figure 14. ADC input impedance equivalency diagram**

3.6.1.2 16-bit ADC electrical characteristics

Table 30. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

Table 30. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

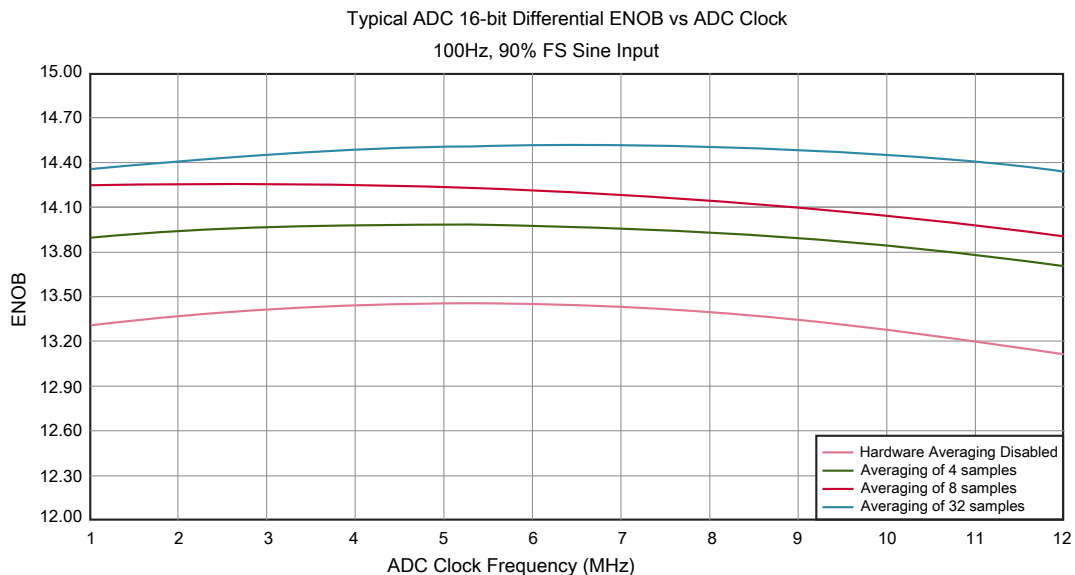
Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	± 4 ± 1.4	± 6.8 ± 2.1	LSB ⁴	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	± 0.7 ± 0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	± 1.0 ± 0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
E_Q	Quantization error	• 16-bit modes • ≤ 13 -bit modes	— —	-1 to 0 —	— ± 0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode					6
		• Avg = 32	12.8	14.5	—	bits	
		• Avg = 4	11.9	13.8	—	bits	
		16-bit single-ended mode					
• Avg = 32	12.2	13.9	—	bits			
• Avg = 4	11.4	13.1	—	bits			
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode				dB	7
		• Avg = 32	—	-94	—	dB	
		16-bit single-ended mode					
		• Avg = 32	—	-85	—		
SFDR	Spurious free dynamic range	16-bit differential mode	82	95	—	dB	7
		• Avg = 32			—	dB	
		16-bit single-ended mode	78	90			

Table continues on the next page...

Table 30. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
		• Avg = 32					
E_{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

**Figure 15. Typical ENOB vs. ADC_CLK for 16-bit differential mode**

Peripheral operating requirements and behaviors

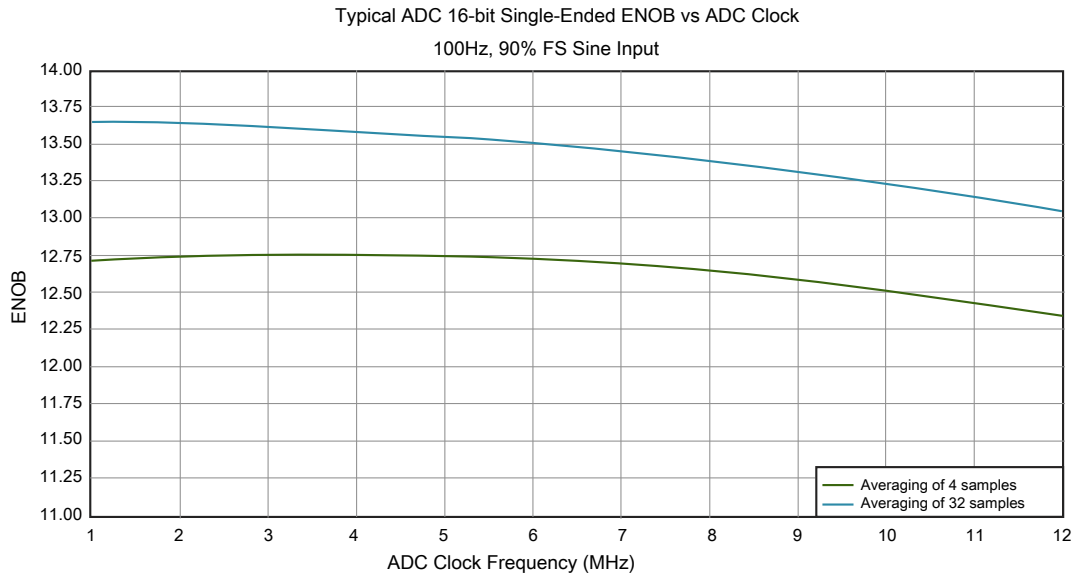


Figure 16. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 31. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μ A
I_{DDL5}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μ A
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 	—	5 10 20 30	—	mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

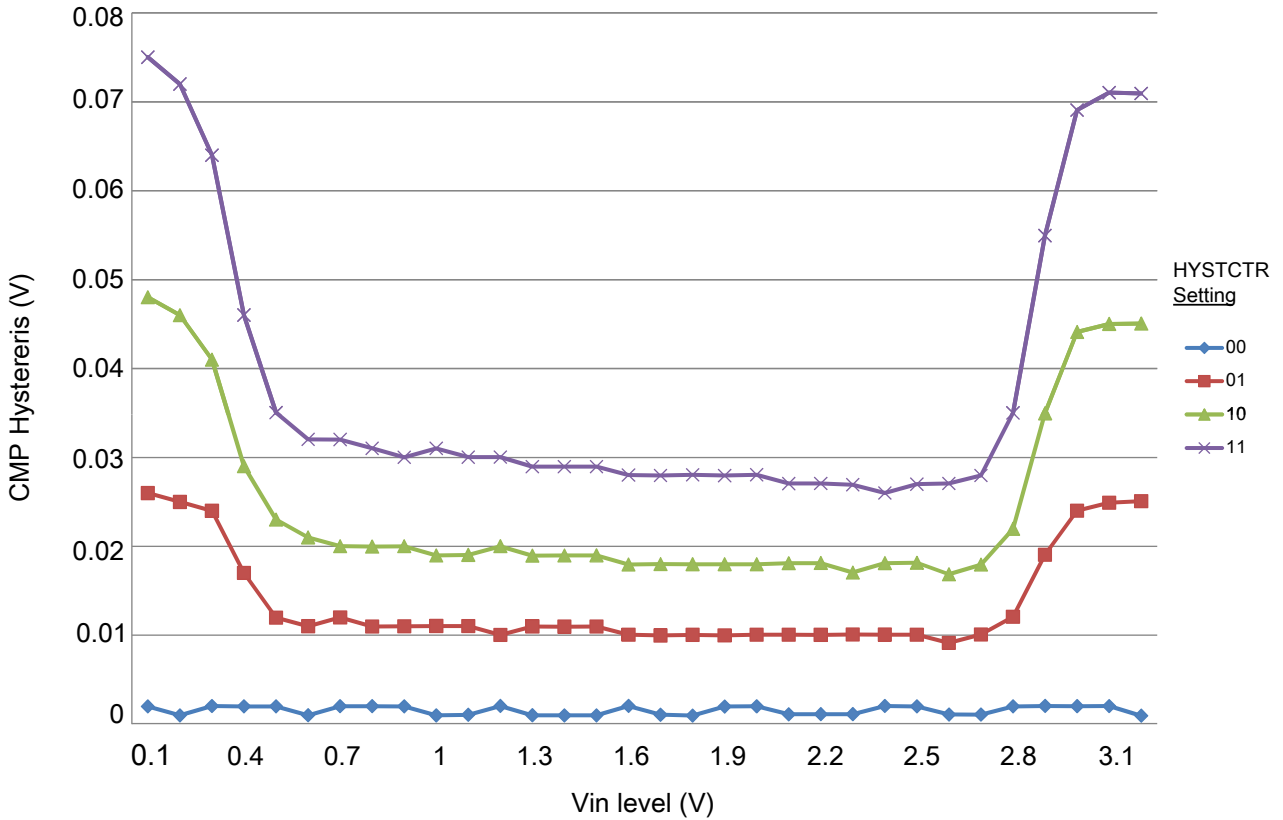


Figure 17. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)



Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 32. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	1200	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
R_{op}	Output resistance (load = 3 k Ω)	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	1.2 0.05	1.7 0.12	— —	$\text{V}/\mu\text{s}$	
BW	3dB bandwidth <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) 	550 40	— —	— —	kHz	

- Settling within ± 1 LSB
- The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
- $V_{DDA} = 3.0\text{ V}$, reference select set for V_{DDA} ($DACx_CO:DACRFS = 1$), high power mode ($DACx_CO:LPEN = 0$), DAC set to 0x800, temperature range is across the full range of the device

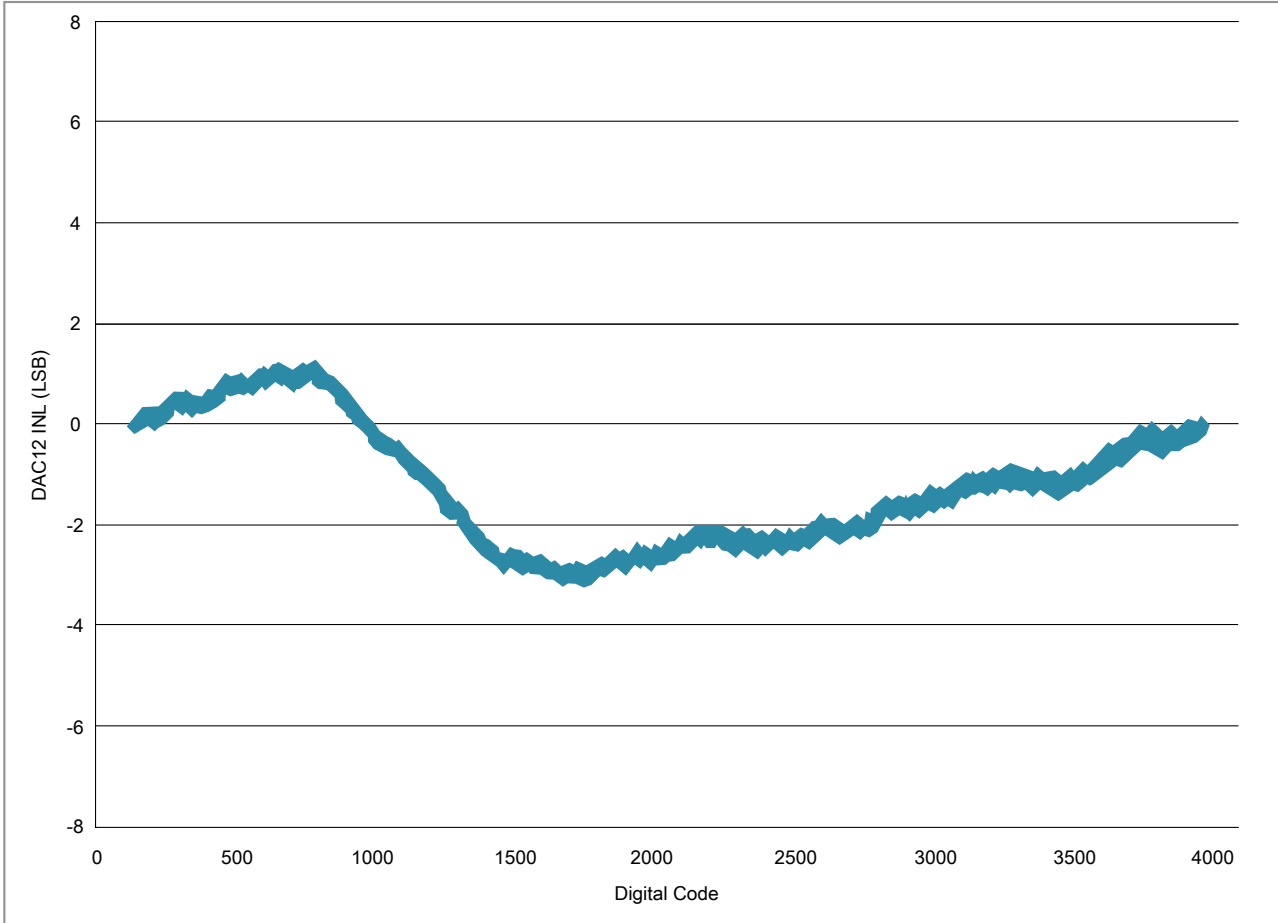


Figure 19. Typical INL error vs. digital code



Figure 20. Offset at half scale vs. temperature

3.6.4 Voltage reference electrical specifications

Table 34. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 35. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25°C	1.1920	1.1950	1.1980	V	1
V_{out}	Voltage reference output with user trim at nominal V_{DDA} and temperature=25°C	1.1945	1.1950	1.1955	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	15	mV	1
I_{bg}	Bandgap only current	—	—	80	μ A	
I_{lp}	Low-power buffer current	—	—	360	μ A	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	μ V	1, 2
T_{stup}	Buffer startup time	—	—	100	μ s	
$T_{chop_osc_st\ up}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	
V_{vdrift}	Voltage drift ($V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 36. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	70	°C	

Table 37. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the limited temperature range)	—	10	mV	

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The MCGPLLCLK meets the USB jitter specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The MCGFLLCLK does not meet the USB jitter specifications for certification.

The IRC48M meets the USB jitter specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB jitter specifications for certification in Host mode operation.

3.8.2 USB VREG electrical specifications

Table 38. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	μA	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I _{DDoff}	Quiescent current — Shutdown mode <ul style="list-style-type: none"> • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature 	—	650	—	nA	
		—	—	4	μA	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V <ul style="list-style-type: none"> • Run mode • Standby mode 	3	3.3	3.6	V	
		2.1	2.8	3.6	V	

Table continues on the next page...

Table 38. USB VREG electrical specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I _{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.8.3 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 39. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 × t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCS _n valid to DSPI_SCK delay	(t _{BUS} × 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS _n invalid delay	(t _{BUS} × 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARN[PSSCK] and SPIx_CTARN[CSSCK].

2. The delay is programmable in SPIx_CTARN[PASC] and SPIx_CTARN[ASC].

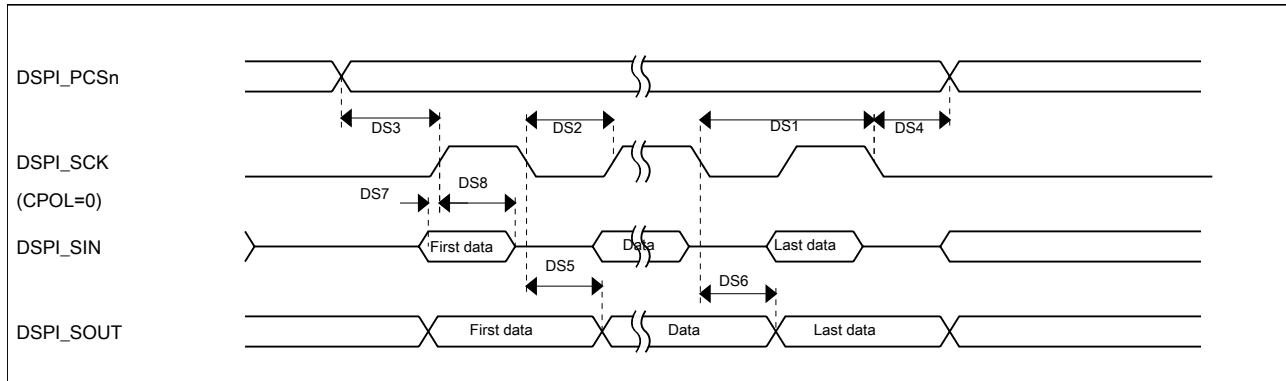


Figure 21. DSPI classic SPI timing — master mode

Table 40. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	15	MHz	1
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns	
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns	
DS15	$\overline{DSPI_SS}$ active to DSPI_SOUT driven	—	17	ns	
DS16	$\overline{DSPI_SS}$ inactive to DSPI_SOUT not driven	—	17	ns	

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

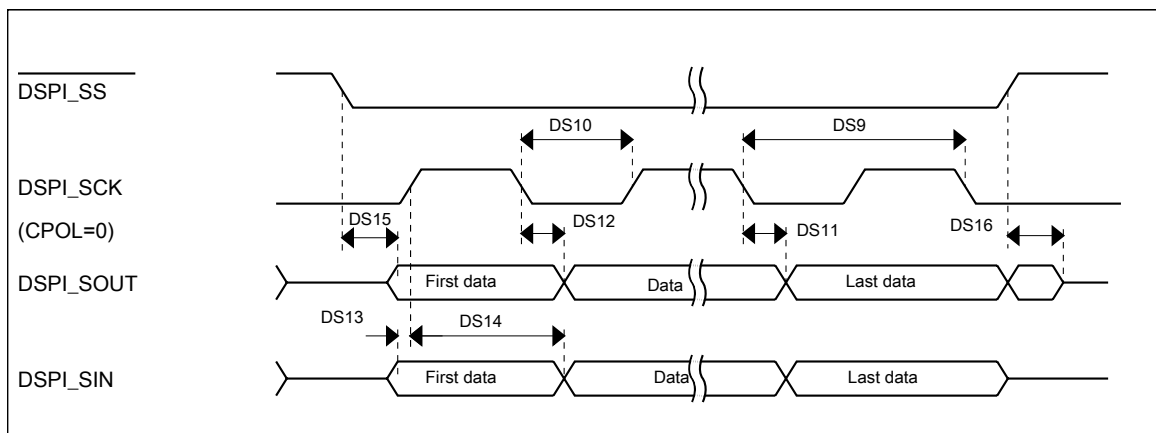


Figure 22. DSPI classic SPI timing — slave mode

3.8.4 DSPI switching specifications (full voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 41. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24.6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

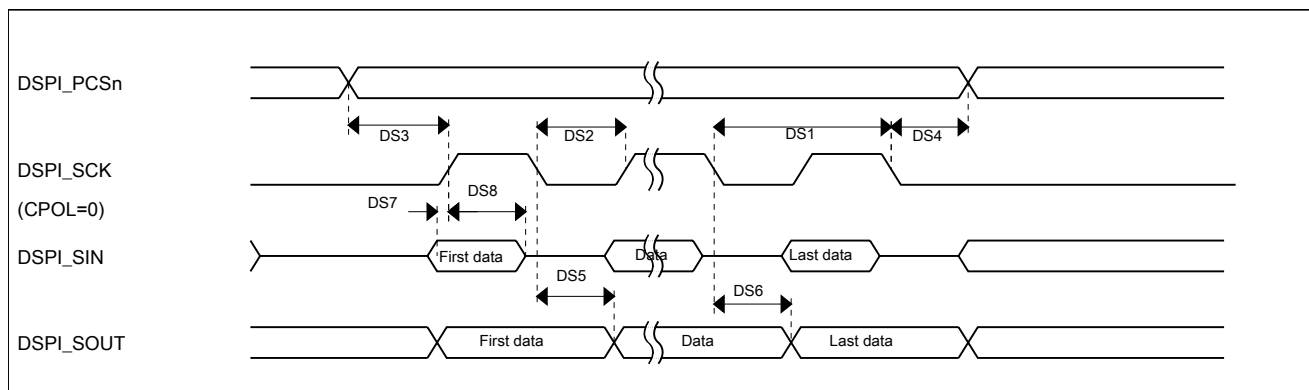


Figure 23. DSPI classic SPI timing — master mode

Table 42. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns

**Figure 24. DSPI classic SPI timing — slave mode**

3.8.5 Inter-Integrated Circuit Interface (I²C) timing

Table 43. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD} ; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t_{SU} ; STA	4.7	—	0.6	—	μs

Table continues on the next page...

Table 43. I²C timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Data hold time for I ² C bus devices	t _{HD} ; DAT	0 ²	3.45 ³	0 ⁴	0.9 ²	μs
Data set-up time	t _{SU} ; DAT	250 ⁵	—	100 ^{3, 6}	—	ns
Rise time of SDA and SCL signals	t _r	—	1000	20 + 0.1C _b ⁷	300	ns
Fall time of SDA and SCL signals	t _f	—	300	20 + 0.1C _b ⁶	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t _{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 44. I²C 1 Mbps timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f _{SCL}	0	1 ¹	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	0.26	—	μs
LOW period of the SCL clock	t _{LOW}	0.5	—	μs
HIGH period of the SCL clock	t _{HIGH}	0.26	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	0.26	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0	—	μs
Data set-up time	t _{SU} ; DAT	50	—	ns
Rise time of SDA and SCL signals	t _r	20 + 0.1C _b ²	120	ns
Fall time of SDA and SCL signals	t _f	20 + 0.1C _b ²	120	ns
Set-up time for STOP condition	t _{SU} ; STO	0.26	—	μs
Bus free time between STOP and START condition	t _{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

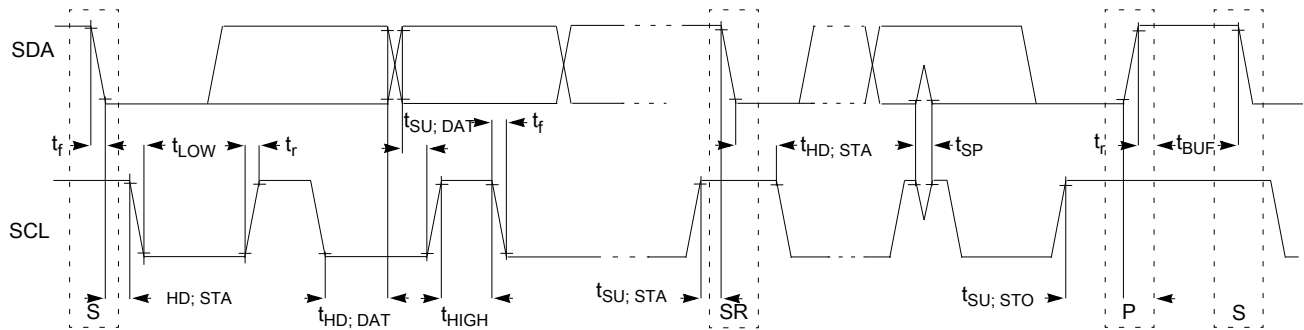


Figure 25. Timing definition for devices on the I²C bus

3.8.6 UART switching specifications

See [General switching specifications](#).

3.8.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

3.8.7.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Table 45. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period

Table continues on the next page...

Table 45. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	18	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

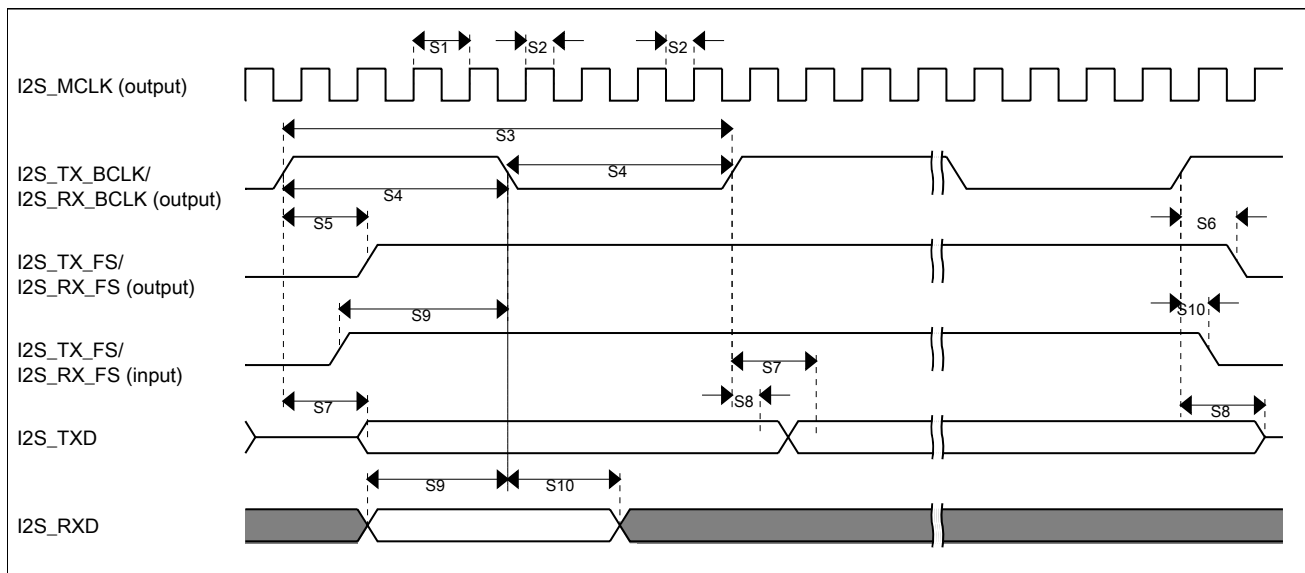


Figure 26. I2S/SAI timing — master modes

Table 46. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

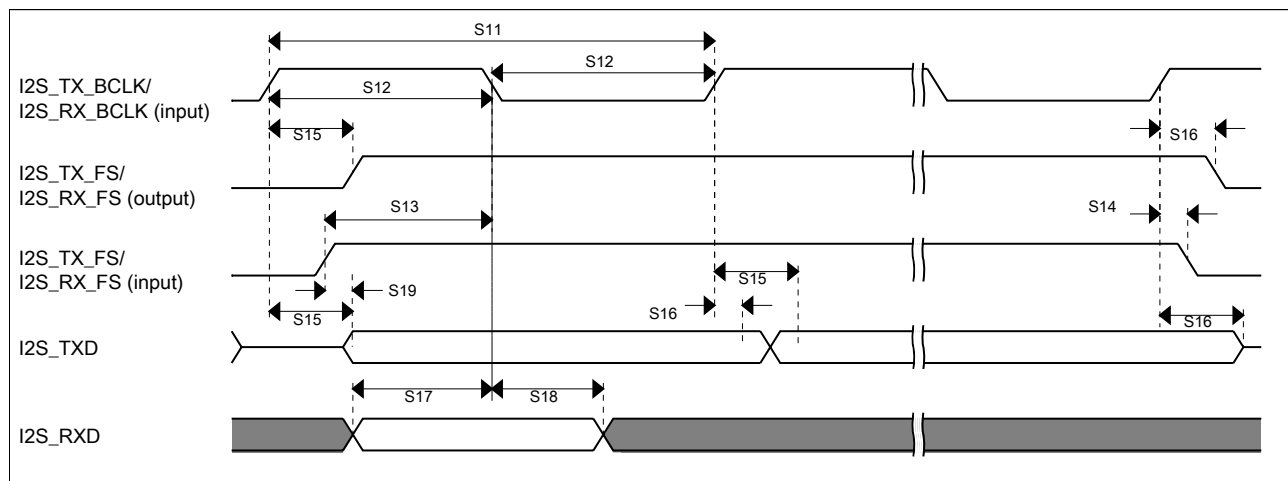
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns

Table continues on the next page...

Table 46. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	20	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

**Figure 27. I2S/SAI timing — slave modes**

3.8.7.2 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 47. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period

Table continues on the next page...

Table 47. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	27	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

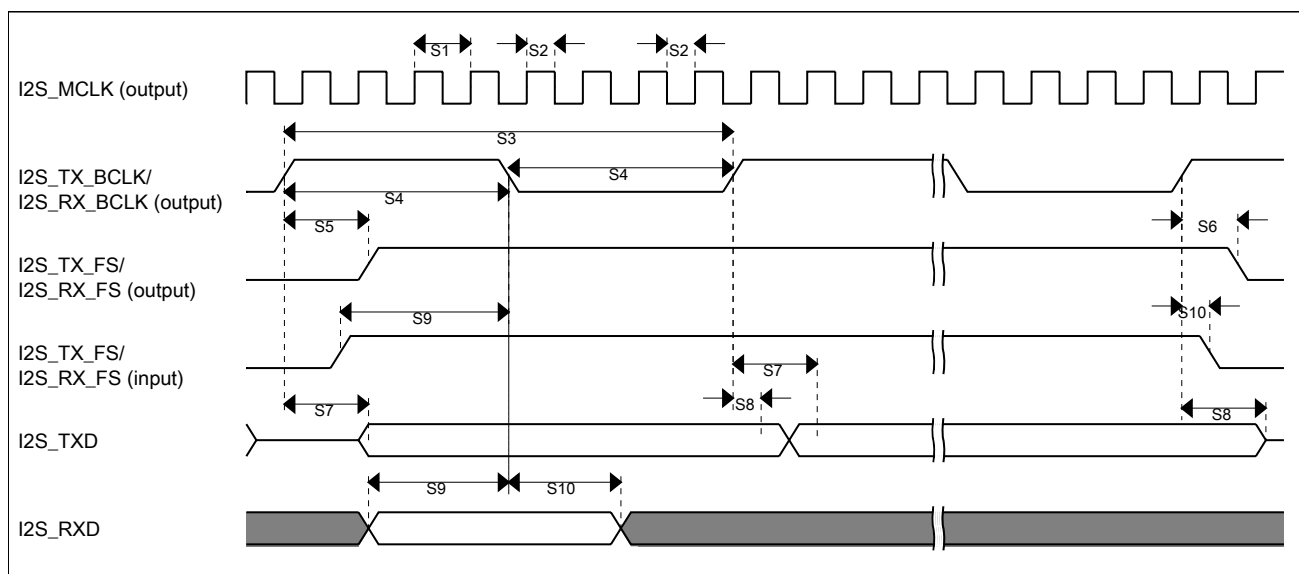


Figure 28. I2S/SAI timing — master modes

Table 48. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

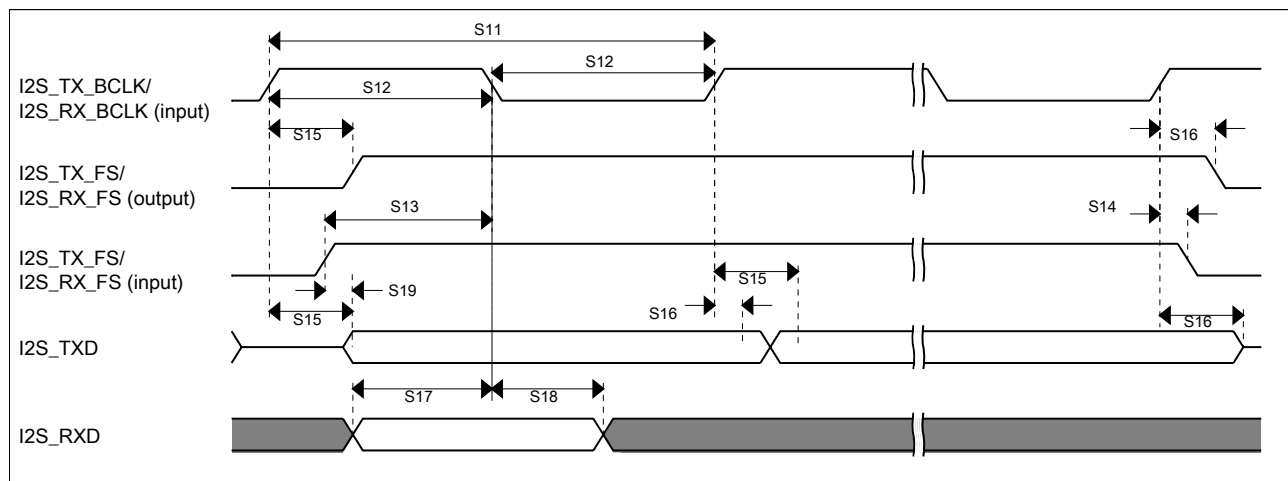
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns

Table continues on the next page...

Table 48. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	28.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	26.3	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

**Figure 29. I2S/SAI timing — slave modes**

3.8.7.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 49. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period

Table continues on the next page...

Table 49. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

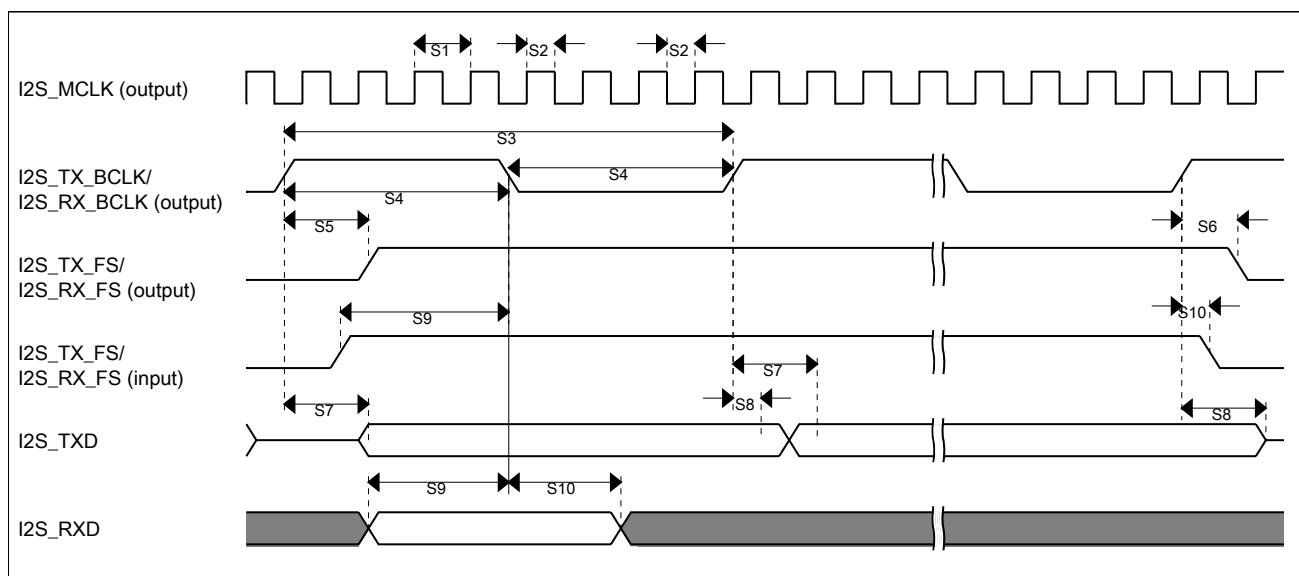


Figure 30. I2S/SAI timing — master modes

Table 50. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

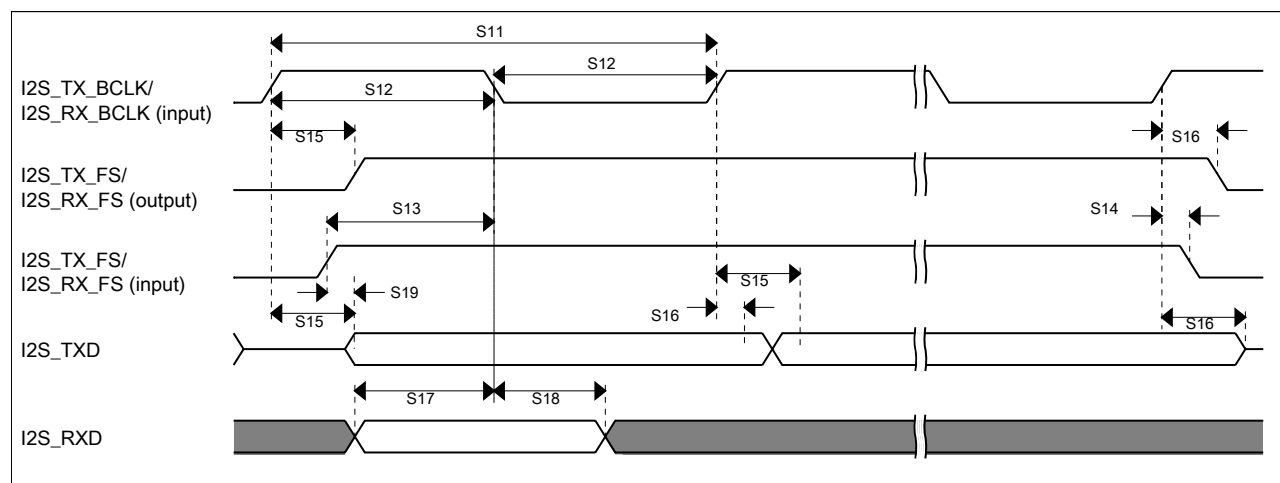
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7	—	ns

Table continues on the next page...

Table 50. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	4	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

**Figure 31. I2S/SAI timing — slave modes**

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
80-pin WLCSP (AP)	98ASA00710D
80-pin WLCSP (BP)	98ASA00820D

5 Pinout

5.1 K22F Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. This table applies to both the standard and the thin height packages. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

80 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E7	PTE0/ CLKOUT32K	ADC1_SE4a	ADC1_SE4a	PTE0/ CLKOUT32K	SPI1_PCS1	UART1_TX			I2C1_SDA	RTC_ CLKOUT	
A8	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			I2C1_SCL	SPI1_SIN	
A9	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b					
A10	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b				SPI1_SOUT	
B8	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	LPUART0_TX					
C8	PTE5	DISABLED		PTE5	SPI1_PCS2	LPUART0_RX			FTM3_CH0		
B9	VDD	VDD	VDD								
B10	VSS	VSS	VSS								
D8	VSS	VSS	VSS								
C10	USB0_DP	USB0_DP	USB0_DP								
D10	USB0_DM	USB0_DM	USB0_DM								
C9	VOUT33	VOUT33	VOUT33								
D9	VREGIN	VREGIN	VREGIN								
E10	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2								
F10	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2								
E9	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3								
F9	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3								
G9	VDDA	VDDA	VDDA								
G10	VREFH	VREFH	VREFH								
H10	VREFL	VREFL	VREFL								
H9	VSSA	VSSA	VSSA								

80 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E8	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
F8	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
G7	RTC_WAKEUP_B	RTC_WAKEUP_B	RTC_WAKEUP_B								
G8	XTAL32	XTAL32	XTAL32								
H8	EXTAL32	EXTAL32	EXTAL32								
H7	VBAT	VBAT	VBAT								
F7	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
F6	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
F5	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
F4	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
G6	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
H5	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2			I2S0_TX_BCLK	JTAG_TRST_b	
H6	PTA12	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_PHA	
H4	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_PHB	
G5	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_BCLK		
G4	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
H3	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b			I2S0_RX_FS		
G3	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		
E6	VDD	VDD	VDD								
G2	VSS	VSS	VSS								
H2	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
H1	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
G1	RESET_b	RESET_b	RESET_b								

Pinout

80 WLC SP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
F3	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
E3	PTB1	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
F2	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_ b			FTM0_FLT3		
F1	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_ b			FTM0_FLT0		
E2	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	LPUART0_RX		FB_AD19	FTM0_FLT1		
E1	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	LPUART0_TX		FB_AD18	FTM0_FLT2		
E4	VSS	VSS	VSS								
D5	VDD	VDD	VDD								
D1	PTB16	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0	FB_AD17	EWM_IN		
D2	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1	FB_AD16	EWM_OUT_b		
D3	PTB18	DISABLED		PTB18		FTM2_CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_QD_ PHA		
D4	PTB19	DISABLED		PTB19		FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB		
C1	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_ EXTRG	USB_SOF_ OUT	FB_AD14			
B1	PTC1/ LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0	FB_AD13	I2S0_TXD0	LPUART0_ RTS_b	
C2	PTC2	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1	FB_AD12	I2S0_TX_FS	LPUART0_ CTS_b	
C3	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK	LPUART0_RX	
E5	VSS	VSS	VSS								
D6	VDD	VDD	VDD								
A1	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT	LPUART0_TX	
B2	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT	FTM0_CH2	
A2	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9	I2S0_MCLK		
B3	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS	FB_AD8			
A3	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7			
C4	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_ BCLK	FB_AD6	FTM2_FLT0		
B4	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5			
A4	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7		FB_RW_b			

80 WLCSP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B5	PTC16	DISABLED		PTC16		LPUART0_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_ 16_BLS15_8_ b			
A5	PTC17	DISABLED		PTC17		LPUART0_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_ 24_BLS7_0_b			
C5	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b	LPUART0_ RTS_b		
B6	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b	FTM3_CH1	FB_CS0_b	LPUART0_ CTS_b		
A6	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4	LPUART0_RX	I2C0_SCL	
C6	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3	LPUART0_TX	I2C0_SDA	
B7	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4	FB_AD2	EWM_IN	SPI1_PCS0	
A7	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b	FTM0_CH5	FB_AD1	EWM_OUT_b	SPI1_SCK	
C7	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
D7	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7		FTM0_FLT1	SPI1_SIN	

5.2 Recommended connection for unused analog and digital pins

The following table shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application.

Table 51. Recommended connection for unused analog interfaces

Pin Type		Short recommendation	Detailed recommendation
Analog/non GPIO	PGAx/ADCx	Float	Analog input - Float
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DACx_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float

Table continues on the next page...

Table 51. Recommended connection for unused analog interfaces (continued)

Pin Type		Short recommendation	Detailed recommendation
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10k Ω pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
USB	USB0_DP	Float	Float
USB	USB0_DM	Float	Float
USB	VOOUT33	Tie to input and ground through 10k Ω	Tie to input and ground through 10k Ω
USB	VREGIN	Tie to output and ground through 10k Ω	Tie to output and ground through 10k Ω
VBAT	VBAT	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K22 Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	
A	PTC4/ LLWU_P8	PTC6/ LLWU_P10	PTC8	PTC11/ LLWU_P11	PTC17	PTD2/ LLWU_P13	PTD5	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTE3	A
B	PTC1/ LLWU_P6	PTC5/ LLWU_P9	PTC7	PTC10	PTC16	PTD1	PTD4/ LLWU_P14	PTE4/ LLWU_P2	VDD	VSS	B
C	PTC0	PTC2	PTC3/ LLWU_P7	PTC9	PTD0/ LLWU_P12	PTD3	PTD6/ LLWU_P15	PTE5	VOUT33	USB0_DP	C
D	PTB16	PTB17	PTB18	PTB19	VDD	VDD	PTD7	VSS	VREGIN	USB0_DM	D
E	PTB11	PTB10	PTB1	VSS	VSS	VDD	PTE0/ CLKOUT32K	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_DP3/ ADC1_DP2/ ADC1_SE18	ADC0_DP0/ ADC1_DP3	ADC1_DP1/ ADC0_DP2	E
F	PTB3	PTB2	PTB0/ LLWU_P5	PTA3	PTA2	PTA1	PTA0	DAC0_OUT7/ CMP1_IN3/ ADC0_SE23	ADC0_DM0/ ADC1_DM3	ADC1_DM1/ ADC0_DM2	F
G	RESET_b	VSS	PTA17	PTA15	PTA14	PTA4/ LLWU_P3	RTC_ WAKEUP_B	XTAL32	VDDA	VREFH	G
H	PTA19	PTA18	PTA16	PTA13/ LLWU_P4	PTA5	PTA12	VBAT	EXTAL32	VSSA	VREFL	H

Figure 32. K22F 80 WLCSP pinout diagram (transparent top view)

6 Part identification

6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

6.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

6.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> M = Fully qualified, general market flow, full reel P = Prequalification K = Fully qualified, general market flow, 100 piece reel
K##	Kinetis family	<ul style="list-style-type: none"> K22
A	Key attribute	<ul style="list-style-type: none"> D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	<ul style="list-style-type: none"> N = Program flash only X = Program flash and FlexMemory
FFF	Program flash memory size	<ul style="list-style-type: none"> 128 = 128 KB 256 = 256 KB 512 = 512 KB
R	Silicon revision	<ul style="list-style-type: none"> Z = Initial (Blank) = Main A = Revision after main
T	Temperature range (°C)	<ul style="list-style-type: none"> C = -40 to 85
PP	Package identifier	<ul style="list-style-type: none"> AP = 80 WLCSP (4.13 mm x 3.56 mm x 0.564 mm) BP = 80 WLCSP (4.13 mm x 3.56 mm x 0.321 mm)
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> 12 = 120 MHz
N	Packaging type	<ul style="list-style-type: none"> R = Tape and reel

6.4 Example

This is an example part number:

MK22FN512CAP12R

6.5 80-pin WLCSP part marking

The 80-pin WLCSP package parts follow the part-marking scheme in the following table.

Table 52. 80-pin WLCSP part marking

MK Part number	MK Part Marking
MK22FN512CAP12R	MK22FN512CAP12
MK22FN256CAP12R	MK22FN256CAP12
MK22FN512CBP12R	MK22FN512CBP12

7 Revision History

The following table provides a revision history for this document.

Table 53. Revision History

Rev. No.	Date	Substantial Changes
6	10/2015	<ul style="list-style-type: none"> Throughout: Removed notes related to limited availability of the 80-pin WLCSP (BP) In "Power consumption operating behaviors" section, added "Low power mode peripheral adders—typical value" table In "Thermal operating requirements" table, in footnote, corrected "$T_J = T_A + \Theta_{JA}$" to "$T_J = T_A + R_{\Theta JA}$" Updated "IRC48M specifications" table Updated "NVM program/erase timing specifications" table; removed row for $t_{hversall}$ and added row for $t_{hversblk256k}$ Updated "Flash command timing specifications" table; added rows for $t_{rd1blk256k}$ and $t_{ersblk256k}$ In "Slave mode DSPI timing (limited voltage range)" table, added footnote regarding maximum frequency of operation Added new section, "Recommended connections for unused analog and digital pins"
5	4/2015	Initial public release

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