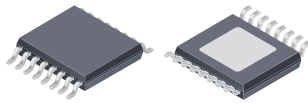# ALT80800

Automotive-Grade, Constant-Current 2.0 A PWM Dimmable Synchronous Buck LED Driver

FEATURES AND BENEFITS

- AEC-Q100 qualified
- Supply voltage 4.5 to 55 V
- 2.0 A maximum output over operating temperature range
- Integrated high-side and low-side MOSFETs: 200 mΩ / 150 mΩ$_{TYP}$
- True average output current control
- Internal control loop compensation
- Integrated 5 V, 14 mA LDO regulator for peripheral circuits
- Dimming via PWM pin or EN pin down to 0.1% at 200 Hz
- Analog dimming (ADIM pin) for brightness calibration and thermal foldback
- Low-power shutdown (1 µA typical)
- Cycle-by-cycle current limit
- Active low fault flag output
- LED open fault mask setting for low V_{IN} operation
- Undervoltage lockout (UVLO) and thermal shutdown protection
- Switching frequency dithering for improved EMC
- Robust protection against:
  □ Adjacent pin-to-pin short
  □ Pin-to-ground short
  □ Component open/short faults

PACKAGE:

16-Pin eTSSOP (suffix LP)

Not to scale

DESCRIPTION

The ALT80800 is a synchronous buck switching regulator that provides constant-current output to drive high-power LEDs. It integrates both high-side and low-side N-channel DMOS switches for DC-to-DC step-down conversion. A true average current is output using a cycle-by-cycle, controlled on-time method.

Output current is user-selectable by an external current sense resistor. Output voltage is automatically adjusted to drive various numbers of LEDs in a single string. This ensures the optimal system efficiency.

LED dimming is accomplished by a direct logic input pulse-width modulation (PWM) signal at the PWM pin while EN is enabled. Alternatively, applying a PWM signal at the EN pin while PWM pin is high can enable "chopped battery" PWM dimming for legacy control modules.

Furthermore, an Analog Dimming input (ADIM pin) can be used, for example, to calibrate the LED current or implement thermal foldback in conjunction with external NTC thermistor.

The ALT80800 is provided in a 16-pin TSSOP (suffix LP), with exposed pad for enhanced thermal dissipation.

APPLICATIONS:

Automotive lighting
• Daytime running lights
• Front and rear fog lights
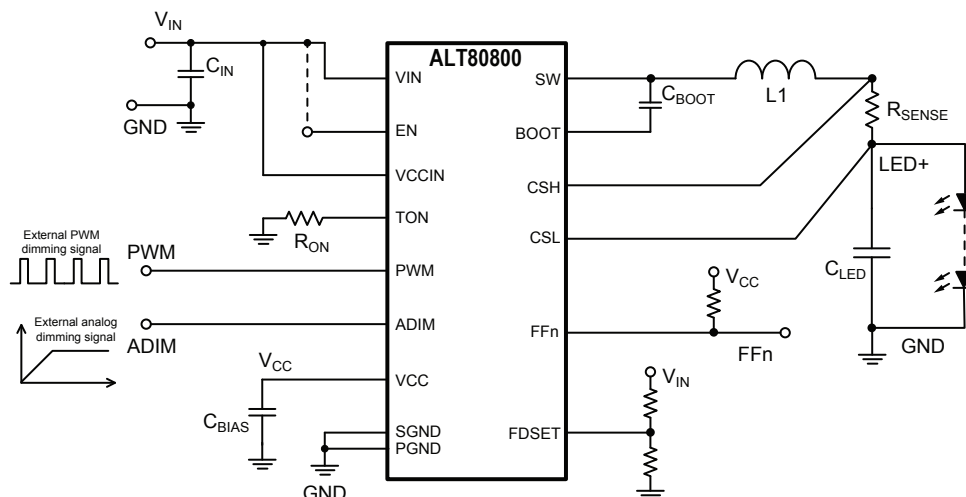• Turn/stop lights
• Map light
• Dimmable interior lights

Figure 1: ALT80800 Typical Application Circuit

Automotive-Grade, Constant-Current 2.0 A PWM Dimmable Synchronous Buck LED Driver

SELECTION GUIDE

Part Number	Package	Packing
ALT80800KLPATR	16-pin TSSOP with exposed thermal pad	4000 pieces per 13-inch reel

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{IN}, V_{VCCIN}		–0.3 to 60	V
Bootstrap Drive Voltage	V_{BOOT}		–0.3 to V_{IN} + 8	V
Switching Voltage	V_{SW}	Continuous	–0.3 to V_{IN} + 0.3	V
		Pulsed, t < 50 ns	–1 to V_{IN} + 3	V
EN Voltage	V_{EN}		–0.3 to V_{IN} + 0.3	V
Current Sense Voltages	V_{CSH}, V_{CSL}			V
Linear Regulator Terminal	V_{CC}		–0.3 to 7	V
ADIM pin, TON pin	V_{ADIM}, V_{TON}			V
FDSET Voltages	V_{FDSET}			V
FFn and PWM Voltages	V_{FFn}, V_{PWM}			V
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS*: May require derating at maximum conditions; see application section for optimization

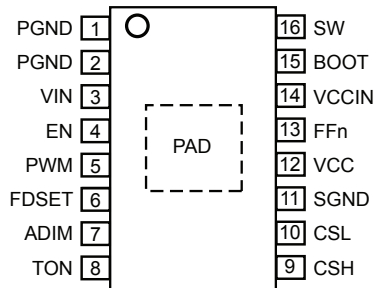| Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	34	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

*Additional thermal information available on the Allegro™ website.

Table of Contents

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PINOUT DIAGRAM AND TERMINAL LIST TABLE

TSSOP-16 (LP) Pinout Diagram

PGND	1		16	SW
PGND	2		15	BOOT
VIN	3		14	VCCIN
EN	4	PAD	13	FFn
PWM	5		12	VCC
FDSET	6		11	SGND
ADIM	7		10	CSL
TON	8		9	CSH

Terminal List Table

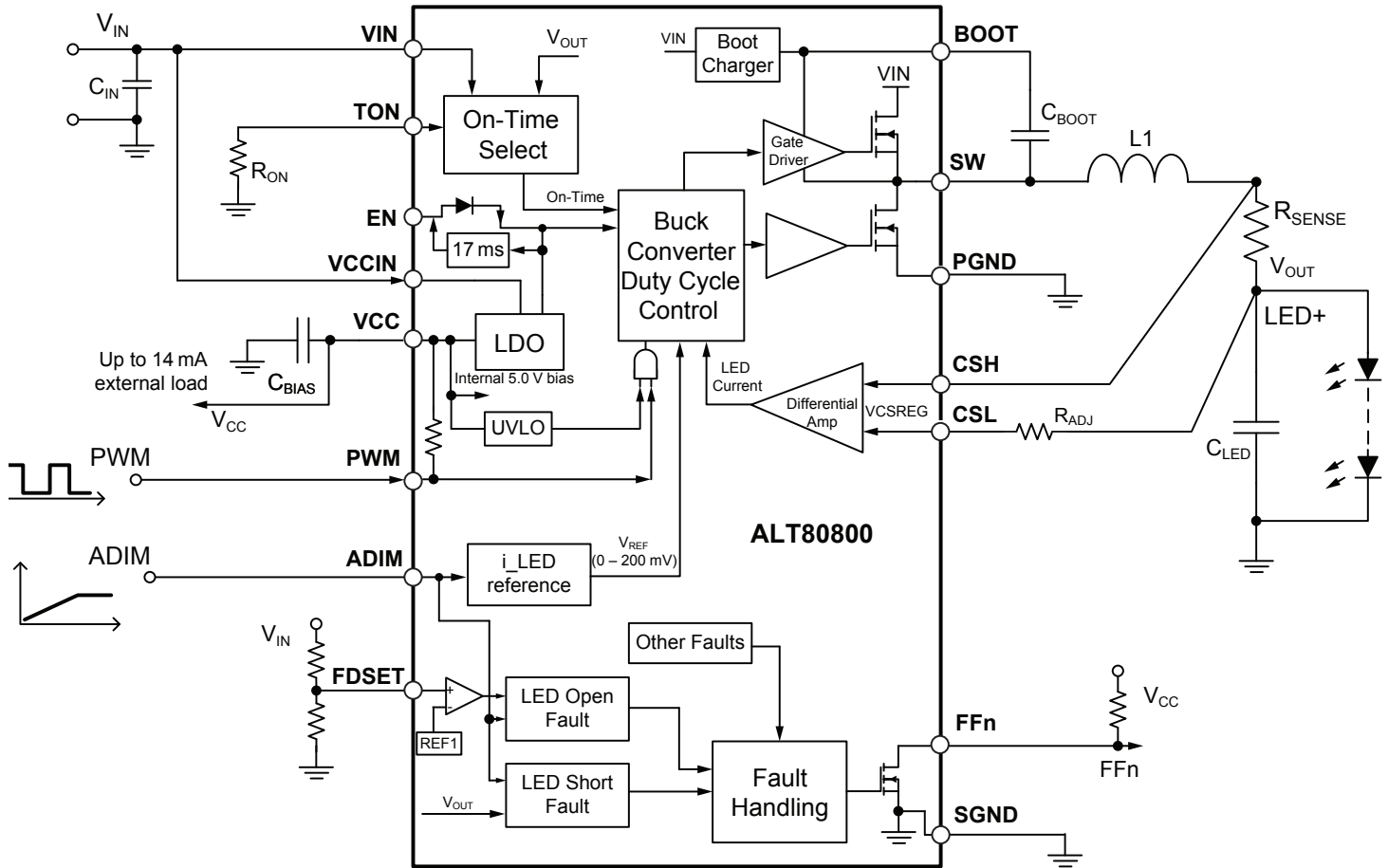| Number	Name	Function
1, 2	PGND	Power ground terminal.
3	VIN	Supply input voltage for power stage.
4	EN	Enable pin for internal LDO regulator and whole IC. EN pin can also be used as PWM dimming when keeping PWM pin High.
5	PWM	Logic input for PWM dimming: when PWM = LOW, LED is off; if PWM = High and at the same time EN is enabled, LED is ON.
6	FDSET	FDSET pin to set the LED Open fault mask threshold. Connect to a voltage divider formed between VIN and PGND. When V_{IN} is low, resulting in FDSET below the internal reference, LED Open Fault detection will be masked.
7	ADIM	Analog dimming control voltage input. If not used for analog dimming, tie ADIM to 5 V or VCC; if used for analog dimming, keep ADIM less than 2.5 V.
8	TON	Regulator on-time setting resistor terminal. Connect a resistor between TON pin and SGND to set the switching frequency.
9	CSH	Current Sense (positive end) feedback input for LED current.
10	CSL	Current Sense (negative end) feedback input for LED current.
11	SGND	Signal ground terminal.
12	VCC	Internal IC bias regulator output. Connect at least 1 µF MLCC to PGND. Can be used to supply up to 14 mA for external load.
13	FFn	Open-drain output which is pulled low in case of fault. Connect through an external pull-up resistor to the desired logic level.
14	VCCIN	It is recommended to connect VCCIN to VIN to bias the internal LDO regulator.
15	BOOT	High-side gate driver bootstrap terminal; a 0.47uF capacitor is recommended between BOOT and SW.
16	SW	Switched output terminal. The output inductor should be connected to this pin.
–	PAD	Exposed pad for enhanced thermal dissipation; connect to ground.

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Figure 2: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at V_{IN} = 12 V, V_{OUT} = 6 V, T_J = –40°C to 125°C, typical values at T_J = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Supply Voltage	V_{IN}		4.5	–	55	V
V_{IN} Undervoltage Lockout Threshold	$V_{UVLO(ON)}$	V_{IN} increasing, V_{IN} = V_{VCCIN}, I_{CC} = 0 mA	–	–	4.3	V
V_{IN} Undervoltage Lockout Hysteresis	$V_{UVLO(HYS)}$	V_{IN} decreasing, V_{IN} = V_{VCCIN}, I_{CC} = 0 mA	100	–	300	mV
VIN Pin Supply Current	I_{IN}	$V_{CSH} - V_{CSL}$ = 0.5 V, V_{EN} = V_{IH_EN}, V_{PWM} = V_{IH_PWM}, R_{ON} = 402 kΩ	–	5	–	mA
VIN Pin Shutdown Current	I_{INSD}	V_{EN} = V_{IL_EN}	–	1	10	µA
Output Current Sense Common Mode Voltage (measured at CSL pin) [1]	V_{OUT}	V_{IN} = 55 V, f_{SW} = 500 kHz, i_{LED} = 0.5 A	2.65	–	50	V
Buck Switch Current Limit Threshold	I_{SWLIM}		2.5	3.25	4.0	A
Buck High-Side Switch On-Resistance	$R_{DSON(HS)}$	V_{BOOT} = V_{IN} + 4.3 V, T_J = 25°C, I_{SW} = 0.5 A	–	0.2	0.32	Ω
Buck Low-Side Switch On-Resistance	$R_{DSON(LS)}$	T_J = 25°C, I_{SW} = 0.5 A	–	0.15	0.24	Ω
BOOT Undervoltage Lockout Threshold	V_{BOOTUV}	V_{BOOT} to V_{SW} increasing	3.1	3.4	3.7	V
BOOT Undervoltage Lockout Hysteresis	$V_{BOTUVHYS}$	V_{BOOT} to V_{SW} decreasing	–	750	–	mV
Switching Minimum Off-Time	t_{OFFmin}	$V_{CSH} - V_{CSL}$ = 0 V	–	100	125	ns
Switching Minimum On-Time	t_{ONmin}		–	65	90	ns
Selected On-Time	t_{ON}	V_{IN} = 12 V, V_{OUT} = 6 V, R_{ON} = 42.2 kΩ	200	–	300	ns
Low-Side Switching Minimum On-Time [2]	t_{LS_ONmin}		–	60	90	ns
t_{ON} Dithering Range	f_{SW_DITH}	R_{ON} = 42.2 kΩ	–	±5%	–	–
Dithering Modulation Frequency	f_{SW_MOD}	R_{ON} = 42.2 kΩ	–	12.5	–	kHz
REGULATION COMPARATOR AND ERROR AMPLIFIER						
Load Current Sense Regulation Threshold at 100% [3]	V_{CSREG}	$V_{CSH} - V_{CSL}$ decreasing, SW turns on, ADIM tied to VCC	194	200	206	mV
CSH Input Sense Current [4]	I_{CSH}	$V_{CSH} - V_{CSL}$ = 0.2 V	–	–250	–	µA
CSL Input Sense Current	I_{CSL}	$V_{CSH} - V_{CSL}$ = 0.2 V	50	75	100	µA
INTERNAL LINEAR REGULATOR						
VCC Regulated Output	V_{CC}	0 mA < I_{CC} < 14 mA, V_{VCCIN} > 6 V	4.85	5.0	5.15	V
VCC Dropout Voltage	V_{LDO}	Measure $V_{VCCIN} - V_{CC}$: V_{VCCIN} = 4.8 V, I_{CC} = 14 mA	–	0.3	0.55	V
VCC Current Limit	i_{VCCLIM}	V_{CC} ≥ 4.35 V	20	–	–	mA
VCC Undervoltage Lockout	V_{CCUVLO}	Rising	3.65	3.9	4.05	V
	$V_{CCUVLOHYS}$	Hysteresis	175	225	275	mV
PWM INPUT						
Logic High Voltage	V_{IH_PWM}	V_{EN} increasing	1.8	–	–	V
Logic Low Voltage	V_{IL_PWM}	V_{EN} decreasing	–	–	1.2	V
PWM Pin Pull-Up Resistance	R_{PWMPU}	V_{CC} = 5 V	–	100	–	kΩ
EN INPUT						
Maximum IC Turn Off Delay	$t_{OFFDelay}$	Measured while PWM dimming signal applied at EN keeping low and exceeding $t_{OFFDelay}$ results in shutdown	10	17	–	ms
Logic High Voltage	V_{IH_EN}	EN increasing	1.8	–	–	V
Logic Low Voltage	V_{IL_EN}	EN decreasing	–	–	0.4	V

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued): Valid at V_{IN} = 12 V, V_{OUT} = 6 V, T_J = –40°C to 125°C, typical values at T_J = 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ANALOG DIMMING INPUT						
Input Voltage for 100% LED Current	V_{ADIMH}	$V_{CSH} – V_{CSL} = V_{CSREG}$	2.1	–	–	V
Regulation Threshold at 50% Analog Dimming	$V_{CSREG50}$	V_{ADIM} = 1.0 V	–	100	–	mV
Regulaton Threshold at 20% Analog Dimming	$V_{CSREG20}$	V_{ADIM} = 0.4 V	38.4	40	41.4	mV
FAULT						
LED Open/Short Detect Condition ADIM Range		V_{ADIM} rising	244	264	284	mV
LED Short Fault Output Voltage Low Threshold		V_{OUT} falling	1.3	1.5	1.7	V
LED Open-Fault Enable Reference	V_{REF1}		2.352	2.4	2.448	V
LED Open Fault Current Threshold	V_{CS_OPEN}	V_{CSREG} = 200 mV start falling (PWM duty = max), $V_{ADIM} = V_{CC}$, $V_{FDSET} = V_{CC}$	(20 mV) 10%	(50 mV) 25%	(80 mV) 40%	–
LED Open Fault Current Hysteresis [1]	$V_{CS\_OPEN\_HYS}$	V_{CSREG} = 200 mV start falling (PWM duty = max), $V_{ADIM} = V_{CC}$, $V_{FDSET} = V_{CC}$	(6 mV) 3%	(12 mV) 6%	(18 mV) 9%	–
Fault Deglitch Timer	t_{FDG}		35	50	65	µs
Fault Mask Timer	t_{MASK}		70	100	130	µs
FFn Pull-Down Voltage	$V_{FAULT(PD)}$	Fault condition asserted, pull-up current = 1 mA	–	–	0.4	V
FFn Pin Leakage Current	$I_{FAULT(LKG)}$	Fault condition cleared, pull-up to 5 V	–	–	1	µA
FFn Rising Time [1]	t_{RISE}	The transition time FFn pin takes from Low to High	–	–	10	µs
FFn Falling Time [1]	t_{FALL}	The transition time FFn pin takes from High to Low	–	–	10	µs
Cool Down Timer for Fault Retry	t_{RETRY}		–	1	–	ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold [1]	T_{SD}		150	165	180	°C
Thermal Shutdown Hysteresis	T_{SDHYS}		–	25	–	°C

[1] Determined by design and characterization. Not production tested.
[2] Guaranteed by design, HS and LS switches are interlocked, as illustrated below:
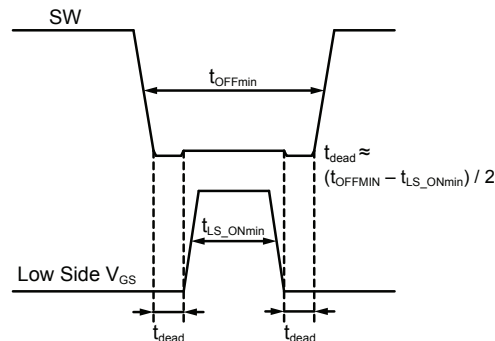
[3] In test mode, a ramp signal is applied between CSH and CSL pins to determine the $V_{CSH} – V_{CSL}$ regulation threshold voltage. In actual application, the average $V_{CSH} – V_{CSL}$ voltage is regulated at V_{CSREG} regardless of ripple voltage.
[4] Negative current is defined as coming out of (sourcing) the specified device pin or node.

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FUNCTIONAL DESCRIPTION

The ALT80800 is a synchronous buck regulator designed for driving a high-current LED string. It uses average current mode control to maintain constant LED current and consistent brightness. The LED current level is easily programmable by selection of an external sense resistor, with a value determined as follows:

$$i_{LED} = V_{CSREG} / R_{SENSE}$$

where $V_{CSREG} = V_{CSH} - V_{CSL} = 0.2$ V typical.

If necessary, a resistor can be inserted in series with the CSL pin to fine-tune the LED current, as shown below:

$V_{CSREG} = i_{LED} \times R_{SENSE} + i_{CSL} \times R_{adj}$
Therefore
$i_{LED} = (V_{CSREG} - i_{CSL} \times R_{adj}) / R_{SENSE}$
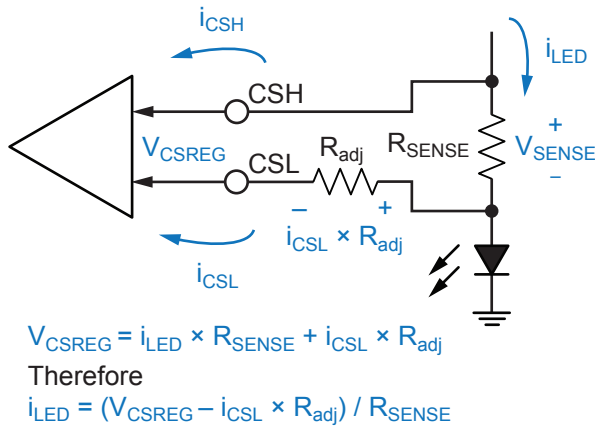
Figure 3: How To Fine-Tune LED Current Using R_{adj}

For example, with a desired LED current of 1.4 A, the required R_{SENSE} = 0.2 V / 1.4 A = 0.143 Ω. But the closest power resistor available is 0.13 Ω. Therefore, the difference is

$$R_{adj} \times i_{CSL} = 0.2\ V - 1.4\ A \times 0.13\ \Omega = 0.018\ V$$

where i_{CSL} = 75 μA typical

$$R_{adj} = 0.018\ V / 75\ \mu A = 240\ \Omega$$

The LED current is further modulated by the ADIM (Analog Dimming) pin voltage. This feature can be used for LED brightness calibration, or for thermal foldback protection. See Analog Dimming section for details.

Synchronous Regulation

The ALT80800 integrates an N-channel DMOS as the low-side switch to implement synchronous regulation for LED drivers, as shown in Figure 4.
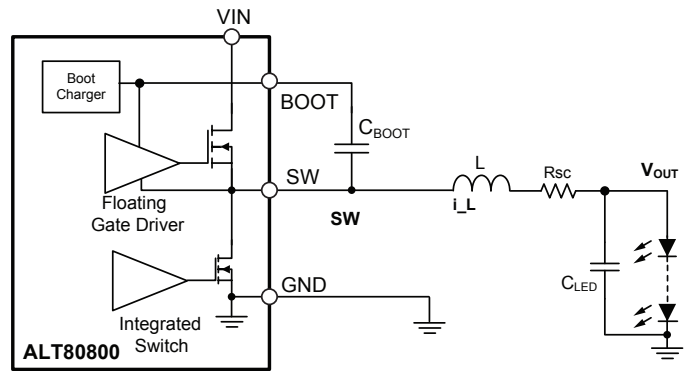

Figure 4: Synchronous Buck LED Driver

The Synchronous configuration can effectively pull down SW to ground by forcing the low-side synchronous switch on even with small inductor current, as shown in Figure 5. Therefore, the BOOT capacitor can be charged normally every switch cycle to ensure the normal operation of buck LED drivers.
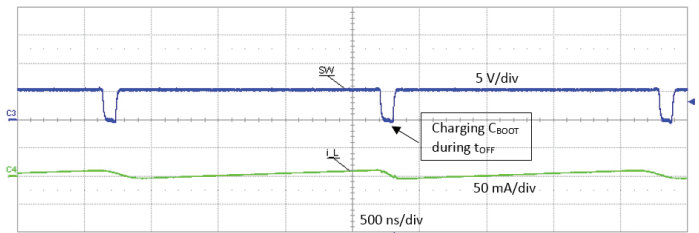

Figure 5: Normal SW waveform with SR configuration when $V_{IN} \approx V_{OUT}$: V_{IN} = 5.4 V, V_{OUT} = 5.14 V (2 white LEDs)

Switching Frequency

The ALT80800 operates in fixed on-time mode during switching. The on-time (and hence switching frequency) is programmed using an external resistor connected between the TON pin and ground, as given by the following equation:

$$t_{ON} = k \times (R_{ON} + R_{INT}) \times (V_{OUT} / V_{IN})$$

$$f_{SW} = 1 / [k \times (R_{ON} + R_{INT})]$$

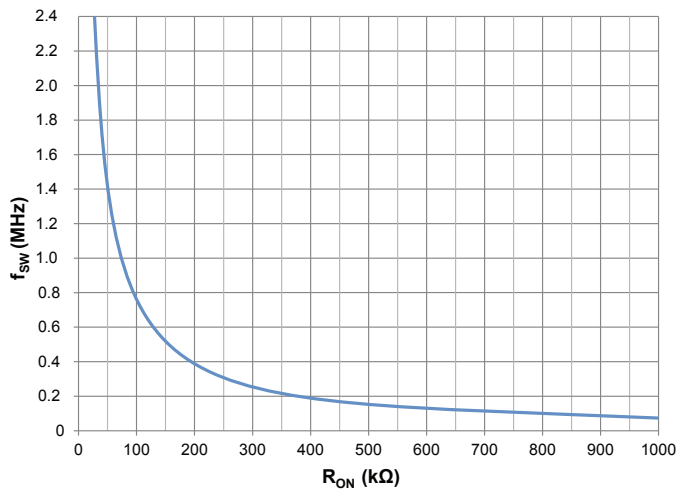where k = 0.0127, with f_{SW} in MHz, t_{ON} in µs, and R_{ON} and R_{INT} (internal resistance, 3 kΩ) in kΩ.

Figure 6: Switching Frequency vs. TON resistance

To minimize the peaks of switching frequency harmonics in EMC measurement, a dithering feature is implemented. The dithering range is internally set at ±5%. The actual switching frequency is swept linearly between $0.95 \times f_{SW}$ and $1.05 \times f_{SW}$, where f_{SW} is the programmed switching frequency. The rate of modulation for f_{SW} is fixed internally at 12.5 kHz.

ENABLE AND DIMMING

The ALT80800 is activated when a logic high signal is applied to the EN (enable) pin and $V_{IN} = V_{VCCIN}$ is above UVLO threshold 4.3 V. The buck converter ramps up the LED current to a target level set by R_{SENSE} when PWM pin = High.

The EN pin is high-voltage tolerant and can be directly connected to a power supply. However, if V_{EN} is higher than the VIN voltage at any time, a series resistor (10 kΩ) is required to limit the current flowing into the EN pin. This resistor is helpful in preventing EN from damage in case of reverse-battery connection. This series

resistor is not necessary if EN is driven from a logic input.

The PWM pin is a logic input pin and is internally pulled up to VCC through a resistor.

EN pin and PWM pin function as illustrated below:

EN pin	PWM pin	VCC	LED
High	Low	ON	OFF
High	High/Open	ON	ON
Low	x	Shutdown	

When the EN pin is forced from high to low, the LED current is turned off, but the IC remains in standby mode for up to at least 10 ms. If EN goes high again within this period, the LED current is turned on immediately if PWM pin is high. If EN pin is low for more than $t_{OFFDelay}$, the IC enters shutdown mode to reduce power consumption. The next high signal on EN will initialize a full startup sequence, which includes a startup delay of approximately 150 µs. This startup delay is not present during PWM operation.

Active dimming of the LED is achieved with 2 options: by sending a PWM (pulse-width modulation) signal to the EN pin (while PWM = High), or by sending a dimming PWM signal to the PWM pin (while EN is enabled) as illustrated in the table above. The resulting LED brightness is proportional to the duty cycle of the applied PWM signal. A practical range for PWM dimming frequency is between 100 Hz (period = 10 ms) and 2 kHz.

If the PWM dimming signal at PWM pin is low when the EN pin is high, the LED will be off immediately and IC is alive waiting for next PWM pulse. The internal LDO is still on and can provide bias to the internal and external circuits.

PWM DIMMING RATIO

The brightness of the LED string can be changed by adjusting the PWM duty cycle at the EN pin as follows:

Dimming ratio = PWM on-time / PWM period

For example, by selecting a PWM period of 5 ms (200 Hz PWM frequency) and a PWM on-time of 5 µs, a dimming ratio of 0.1% can be achieved. This is sometimes referred to as "1000:1 dimming."

In an actual application, the minimum dimming ratio is determined by various system parameters, including: V_{IN}, V_{OUT}, inductance, LED current, switching frequency, PWM frequency, and fault flag usage. The device is easily capable of PWM on-time as short as 5 µs; however, if fault flag for open/short LED detection is required, it should be above 130 µs due to the fault mask timer.

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ANALOG DIMMING

In addition to PWM dimming, the ALT80800 also provides an analog dimming feature. When V_{ADIM} is over 2.0 V, the LED current is at 100% level (as defined by the SENSE resistor). When V_{ADIM} is below 2 V, the LED current decreases linearly down to 20% at V_{ADIM} = 0.4 V. This is shown in the following figure:
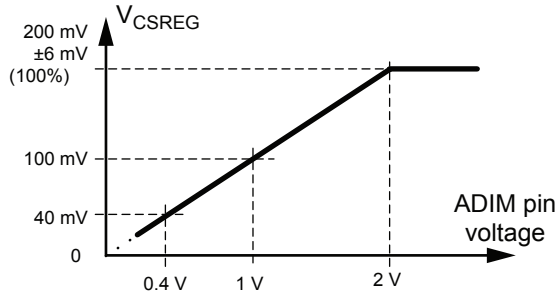

Figure 7: ADIM Pin Voltage Controls SENSE Reference Voltage (hence LED current)

It is possible to pull ADIM pin below 0.4 V to achieve lower than 20% analog dimming. However, if the average LED current determined by ADIM becomes too low and is below half the inductor current ripple, negative current will flow through the inductor. To prevent such cases from happening, it is suggested that ADIM voltage should meet the condition below:

$$ADIM > R_{SENSE} / 0.2 \times (V_{IN} - V_{OUT}) / L \times D \times T$$

where D is duty cycle, $D \approx V_{OUT} / V_{IN}$, T is switching period, $T = 1 / f_{SW}$, L is the inductance.

For example, when R_{SENSE} = 0.2 Ω, R_{ON} = 178 kΩ, L = 33 μH, V_{IN} = 12 V, V_{OUT} = 5.2 V, ADIM voltage should be above 0.21 V, i.e. 11% level, to avoid negative inductor current.

ADIM pin can be used in conjunction with PWM dimming to provide wider LED dimming range over 1000:1. In addition, the IC can provide thermal foldback protection by using an external NTC (negative temperature coefficient) thermistor, as shown below:
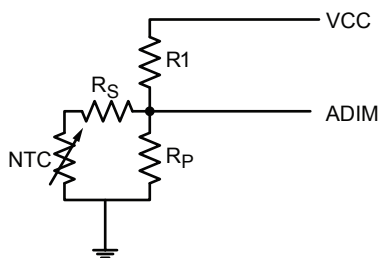

Figure 8: Using an External NTC Thermistor to Implement Thermal Foldback

ADIM is tied to 5 V (or V_{CC}) if never used for analog dimming, or always less than 2.5 V when used for analog dimming. For long term reliability, or extended period with extreme temperature condition, it is better to keep ADIM always less than 2.5 V.

OUTPUT VOLTAGE AND DUTY CYCLE

The figure below provides simplified equations for approximating output voltage. The output voltage of a buck converter is approximately given as:

$$V_{OUT} \approx V_{IN} \times D \, , \, D = t_{ON} / (t_{ON} + t_{OFF})$$
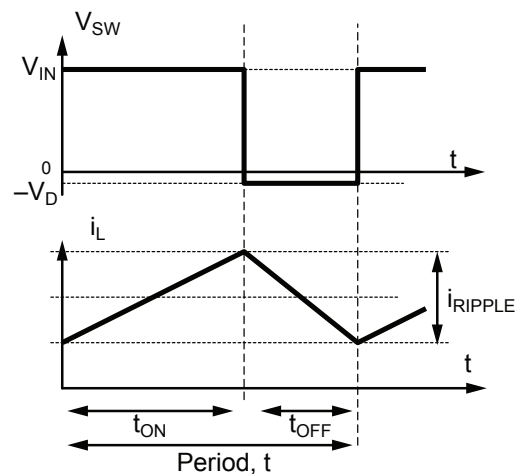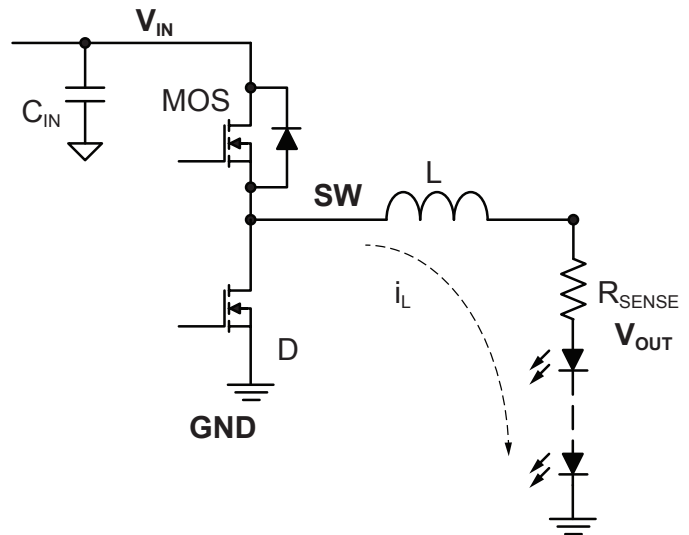
where D is the duty cycle.

Figure 9: Simplified Waveforms for a Buck Converter

During SW on-time:

$$i_{RIPPLE} = (V_{IN} - V_{OUT}) / L \times t_{ON} = (V_{IN} - V_{OUT}) / L \times t \times D$$

where $D = t_{ON} / t$.

During SW off-time:

$$i_{RIPPLE} = V_{OUT} / L \times t_{OFF} = V_{OUT} / L \times t \times (1 - D)$$

Simplified equation for output voltage:

$$V_{OUT} = V_{IN} \times D$$

More precisely:

$$V_{OUT} = (V_{IN} - i_{AVG} \times R_{DSON(HS)}) \times D - (1 - D) \times R_{DSON(LS)} \times i_{AVG} \\ - (DCR + R_{SENSE}) \times i_{AVG}$$

where DCR is the internal resistance of the inductor, R_{SENSE} is the current sensing resistance, $R_{DSON(HS)}$ is the on-resistance of high-side switch, $R_{DSON(LS)}$ is the on-resistance of low-side switch, i_{AVG} is the average current through inductor and equal to LED current.

MINIMUM AND MAXIMUM OUTPUT VOLTAGES

For a given input voltage, the maximum output voltage depends on the switching frequency and minimum t_{OFF}. For example, if t_{OFF}(min) = 100 ns and f_{SW} = 1 MHz, then the maximum duty cycle is 90%. So for an 18 V input, the maximum output is approximately 16.2 V (based on the simplified equation of V_{OUT} = $V_{IN} \times D$). This means up to 5 LEDs can be operated in series, assuming V_f = 3.3 V or less for each LED.

The minimum output voltage depends on minimum t_{ON} and switching frequency. For example, if the minimum t_{ON} = 65 ns and f_{SW} = 1 MHz, then the minimum duty cycle is 6.5%. That means with V_{IN} = 18 V, the theoretical minimum V_{OUT} is just 1.2 V. However, the internal current sense amplifier is designed to guarantee the current accuracy down to V_{OUT} = 2.65 V. When the output voltage is lower than 2.65 V, the regulator keeps switching to regulate, but the current accuracy will suffer and not be guaranteed.

To a lesser degree, the output voltage is also affected by other factors such as LED current, on-resistance of the high-side switch, and DCR of the inductor.

As a general rule, switching at lower frequencies allows a wider range of V_{OUT}, and hence more flexible LED configurations.
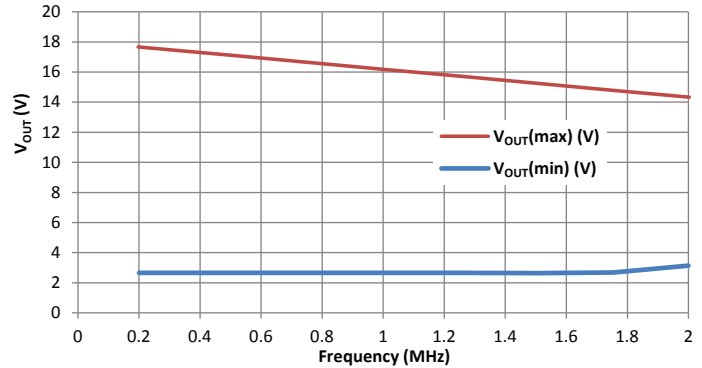

Figure 10: Minimum and Maximum Output Voltage vs. Switching Freqency
(V_{IN} = 18 V, minimum t_{ON} = 90 ns and t_{OFF} = 100 ns)

If the required output voltage is lower than that permitted by the minimum t_{ON}, the controller will automatically extend the t_{OFF} to maintain the correct duty cycle. This means that the switching frequency will drop lower when necessary to keep the LED current in regulation.

If the LED string is completely shorted (V_{OUT} = 0 V), the controller will continue to switch at minimum t_{ON} and will not enter into Hiccup mode.

THERMAL BUDGETING

The ALT80800 is capable of supplying a 2 A current through its high-side switch. However, depending on the duty cycle, the conduction loss in the high-side switch may cause the package to overheat. Therefore care must be taken to ensure the total power loss of package is within budget. For example, if the maximum temperature rise allowed is ΔT = 60°C at the device case surface, then the maximum power dissipation of the IC is 1.75 W. Assuming the maximum $R_{DSON(HS)}$ = 0.32 Ω, $R_{DSON(LS)}$ = 0.24 Ω, and a duty cycle of 70%, then the maximum LED current is limited to 2 A approximately.

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FAULT HANDLING

The ALT80800 is designed to handle the following faults:
• Pin-to-ground short
• Pin-to-neighboring pin short
• Pin open
• External component open or short
• Output short to ground

LED OPEN/OUTPUT SHORT FAULTS

Referring to Fault Function block diagram below, LED Open Fault is masked when V_{IN} is below the pre-set adjustable threshold at FDSET pin or ADIM is below 264 mV. When FDSET is below REF1 or ADIM is below 264 mV with asserting fault flag (FFn = Low), the fault flag keeps asserted if open LED fault exists. Only when FDSET is above REF1 and ADIM is above 264 mV, then the Open fault will be detected by checking current sensing voltage V_{CSREG} and duty cycle. LED Open fault will force regulator into Hiccup mode and assert fault flag, and then fault flag remains asserted during the remaining hiccup mode periods. Once LED open fault disappears, fault flag goes high after hiccup mode period when PWM is high. (refer to Figure 11 and Table 1).
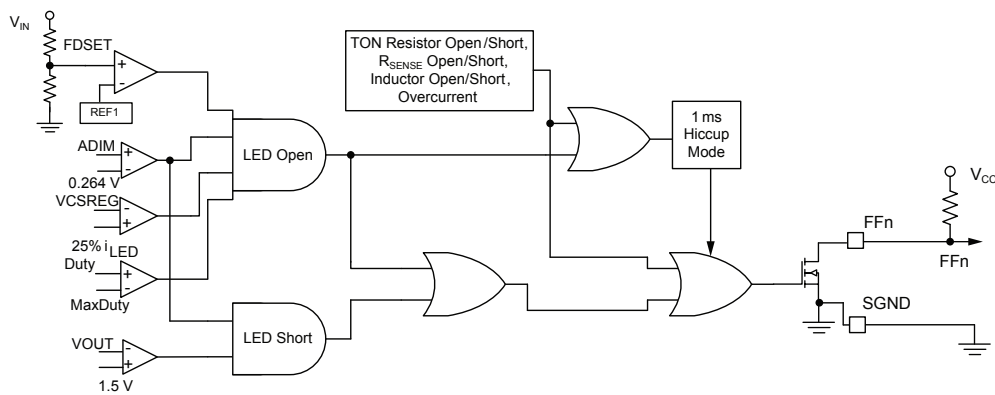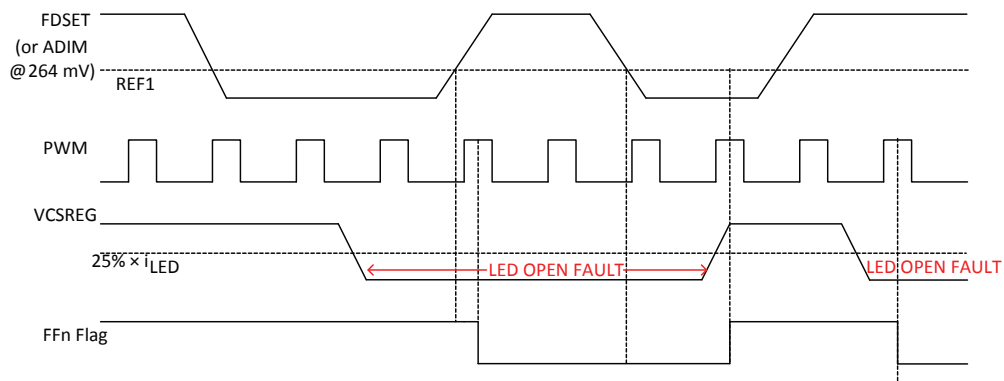
Figure 11a: Simplified Faults Block Diagram

Figure 11b: LED Open Fault Timing Diagram

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Table 1: LED Open Fault Truth Table

FDSET	ADIM	FFn^n	LED Open Fault Event?		PWM	FFn^{n+1}
			$V_{CSREG} < 25\% \times i_{LED}$	Max Duty		
High	High	x	No Open Fault		⤴	1
High	High	x	Yes, Open Fault		⤴	0
Low	x	1	x		x	1
x	Low	1	x		x	1
Low	x	0	Yes, Open Fault		x	0
x	Low	0	Yes, Open Fault		x	0
Low	x	0	No Open Fault		⤴	1
x	Low	0	No Open Fault		⤴	1

FDSET High means FDSET > REF1; FDSET Low means FDSET < REF1;
ADIM High means ADIM > 264 mV; ADIM Low means ADIM < 264 mV

When output Short fault (such as LED shorted to ground or output capacitor shorted to ground) occurs, FFn will be flagged as V_{OUT} drops below 1.5 V and ADIM voltage is above 264 mV; but regulator will not enter into Hiccup mode and will work continuously. When short is removed, ALT80800 will return to normal operation.

When an LED Open/Short fault occurs, the Fault pin will be flagged if the fault remains active after a deglitch period (t_{FDG}). A mask timer (t_{MASK}) is also introduced whenever PWM signal goes from Low to High. During this mask time, faults will not be detected, so the fault will not be detected when the PWM pulse width is less than this mask time. When PWM goes low, fault flag is latched. Fault flag will keep prior state when PWM is Low.

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The Fault deglitch time is fixed; and the Fault mask time is also fixed (refer to Electrical Characteristics table). The LED Open/Short Fault timing diagrams are illustrated below:
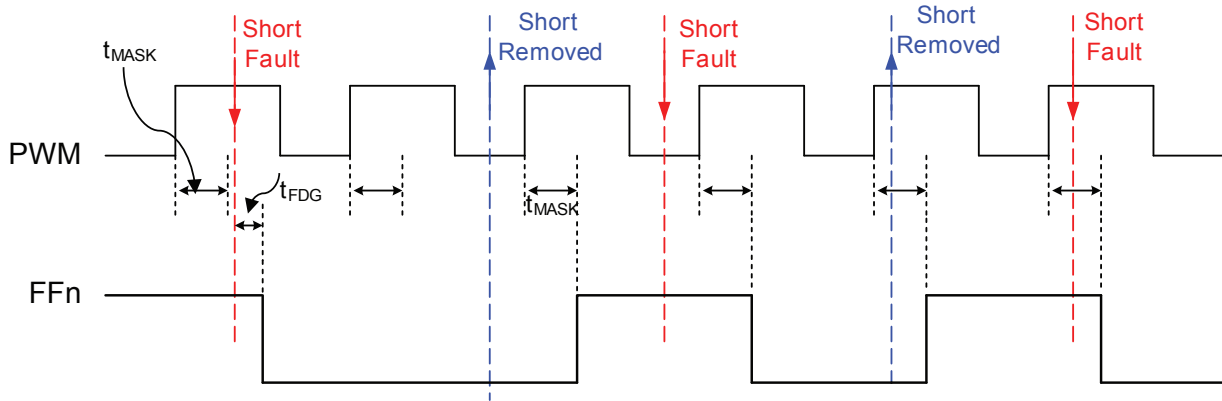
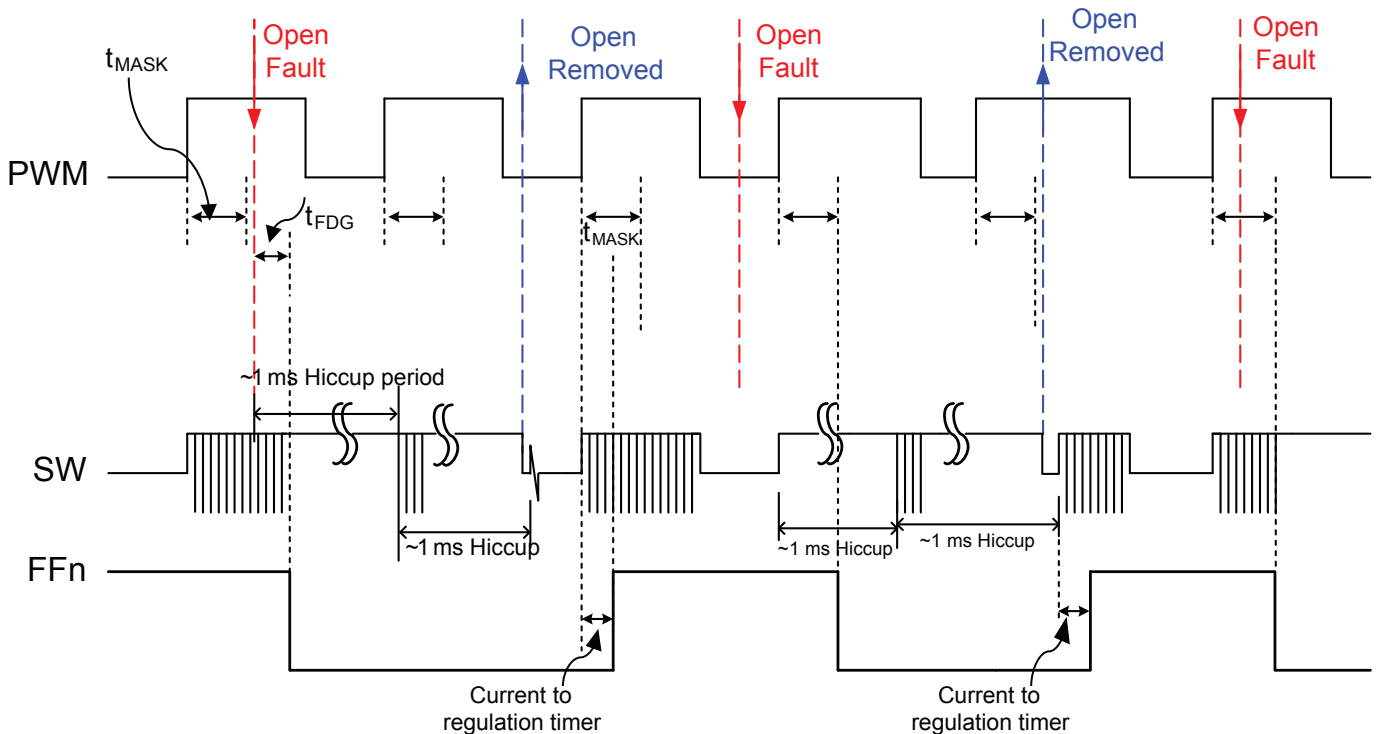

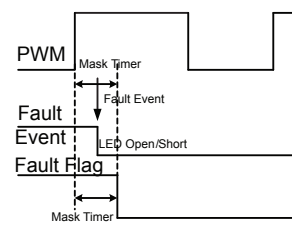**Figure 12a: LED Short Fault Timing Diagram Overview**

Figure 12b: LED Open Fault Timing Diagram Overview

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The basic timing configurations are detailed below for LED Open/Short faults:

Case 1: LED Open/Short Event is outside Mask Timer at PWM = H

PWM
Mask Timer
Fault Event
Fault Event
No LED Fault
LED Open/Short
Fault Flag
Deglitch Timer
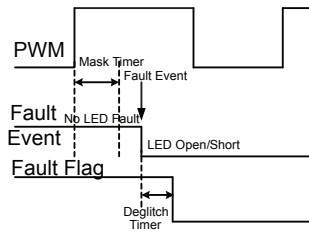
Case 2: LED Open/Short Event is within Mask Timer at PWM = H

PWM
Mask Timer
Fault Event
Fault Event
LED Open/Short
Fault Flag
Mask Timer

Case 3: LED Open/Short Event is close to PWM ↓ at PWM = H

PWM
Mask Timer
Fault Event
Mask Timer
Fault Event
No LED Fault
LED Open/Short
Fault Flag
Mask Timer
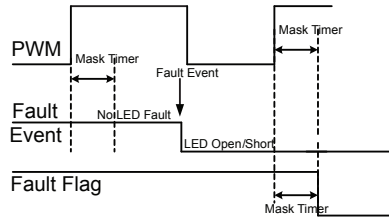
Case 4: LED Open/Short Event is at PWM = L

PWM
Fault Event
Mask Timer
Fault Event
LED Open/Short
Fault Flag
Mask Timer

Case 5: LED Open/Short Removed at PWM = L

a) LED Short Removed at PWM = L

PWM
Mask Timer
Fault Removed
Short Event
No LED Short
Fault Flag
Mask Timer

b) LED Open Removed at PWM = L

PWM
Mask Timer
Fault Removed
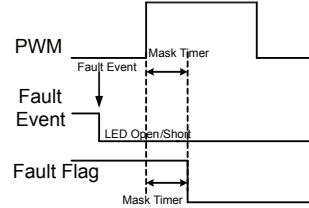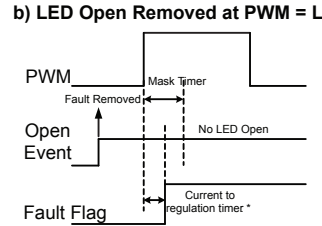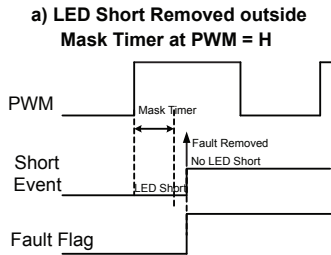Open Event
No LED Open
Fault Flag
Current to regulation timer *
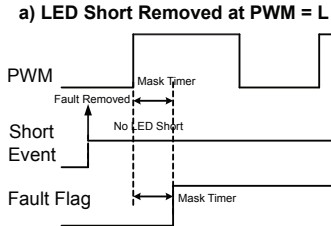
Case 6: LED Open/Short Removed outside Mask Timer at PWM = H

a) LED Short Removed outside Mask Timer at PWM = H

PWM
Mask Timer
Fault Removed
No LED Short
Short Event
LED Short
Fault Flag

b) LED Open Removed outside Mask Timer at PWM = H

PWM
Mask Timer
Fault Removed
No LED Open
Open Event
LED Open
Hiccup period ~1 ms
Fault Flag
Current to regulation timer *
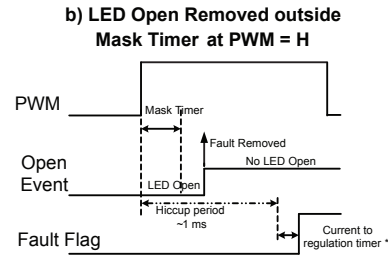
Case 7: LED Open/Short Removed within Mask Timer at PWM = H

a) LED Short Removed within Mask Timer at PWM = H

PWM
Mask Timer
Fault Removed
No LED Short
Short Event
LED Short
Fault Flag

b) LED Open Removed within Mask Timer at PWM=H

PWM
Mask Timer
Fault Removed
No LED Open
Open Event
LED Open
Fault Flag
Current to regulation Timer *
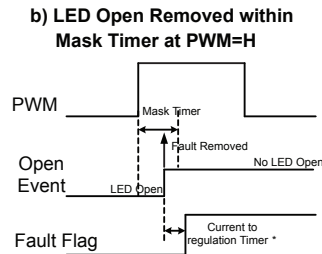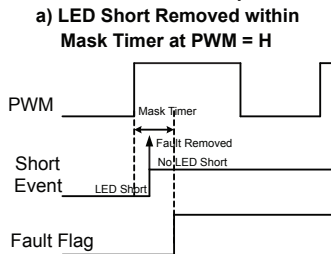
* Current to regulation timer is 256 switching cycles.

SYSTEM FAILURE DETECTION AND PROTECTION DEMONSTRATION

IC-Level Failure Modes
Protected against
- Any pin open
- Any pin shorted to ground
- Adjacent pin-to-pin short

System-Level Failure Modes
Protected against open/short fault for all external components, including:
- LED string
- Sense resistor
- Inductor
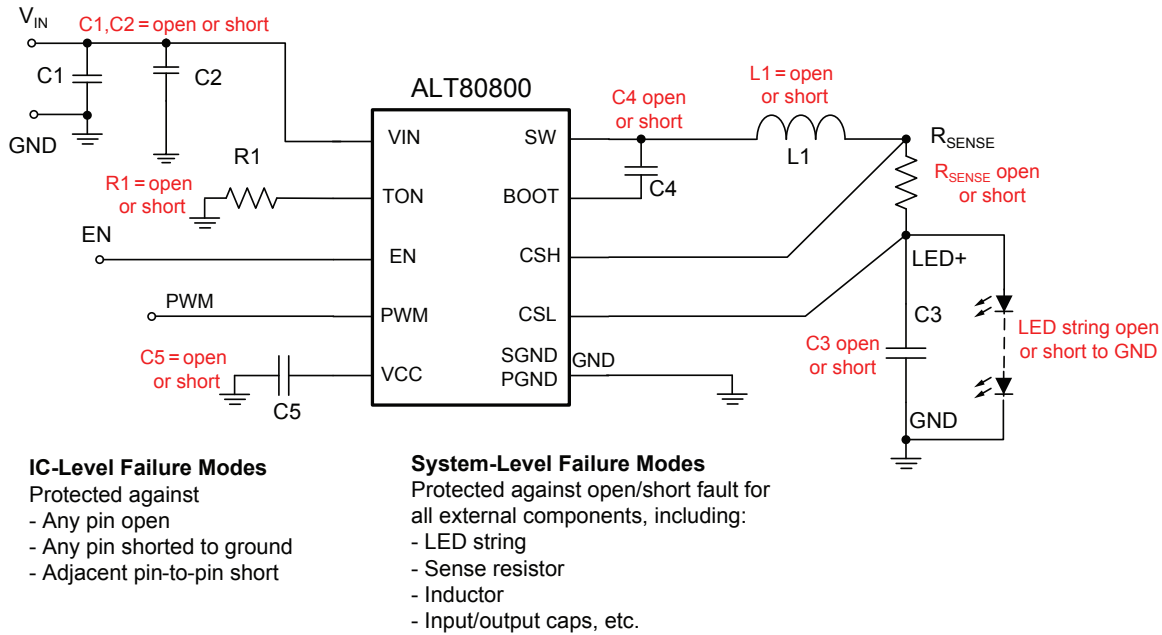- Input/output caps, etc.

Figure 13: Demonstration of various possible fault cases in an application circuit

Table 2: System Failure Mode Table (partial)

| Failure Mode	Symptom Observed	FAULT flag asserted?	ALT80800 Response
Inductor open	Dim light from LED	Yes [1]	When V_{IN} is below preset FDSET setting, regulator switches at maximum duty cycle; when V_{IN} is above FDSET setting, enters into Hiccup mode with 1 ms retry period.
Inductor shorted	Dim light from LED	Yes	Current spike trips SW OCP and turns off switching, entering into Hiccup mode with about 1 ms retry period.
Sense resistor open	Dim light from LED	Yes	High differential sense voltage causes IC to shut off switching, entering into Hiccup mode with about 1 ms retry period.
Sense resistor shorted	Dim light from LED	Yes	Triggers SW OCP fault, entering into Hiccup mode with about 1 ms retry period.
LED string open [1]	No light from LED	Yes [1]	Enter into Hiccup mode with about 1 ms retry period.
LED Strings shorted [2] (Either LED shorted to GND or Output cap shorted to GND) < 1.5 V	Dim light from LED	Yes	Continues switching at minimum TON; regulator will not enter into Hiccup mode.
Output cap open	Normal light from LED	No	Normal operation (since IC only monitors inductor current)
Boot capacitor open	Dim light from LED	Yes	IC attempts to switch but can't fully turn on SW.
Boot capacitor shorted	No light from LED	No	IC detects undervoltage fault across BOOT capacitor and will not start switching.
TON resistor open	Dim light from LED	Yes	Enter into Hiccup mode with about 1 ms retry period.
TON resistor shorted	Dim light from LED	Yes	Enter into Hiccup mode with about 1 ms retry period.

[1] For LED Open Fault, fault flag will not be asserted when V_{IN} is below preset mask threshold, ADIM is below 0.264 V or PWM dimming pulse width is below fault mask timer.

[2] For LED Short Fault, fault flag will not be asserted when ADIM is below 0.264 V or PWM dimming pulse width is below fault mask timer.

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CLAMP DIODES FOR LED OPEN/SHORT PROTECTION

Refer to Figure 14. It is recommended to add clamp diode D1 to provide LED short protection when V_{IN} is above 40 V; if V_{IN} is below 40 V, D1 is not needed. Diode D2 is needed to clamp the overshoot from L-C resonance due to LED Open fault when V_{IN} is above 45 V; when V_{IN} is below 45 V, D2 is not required.
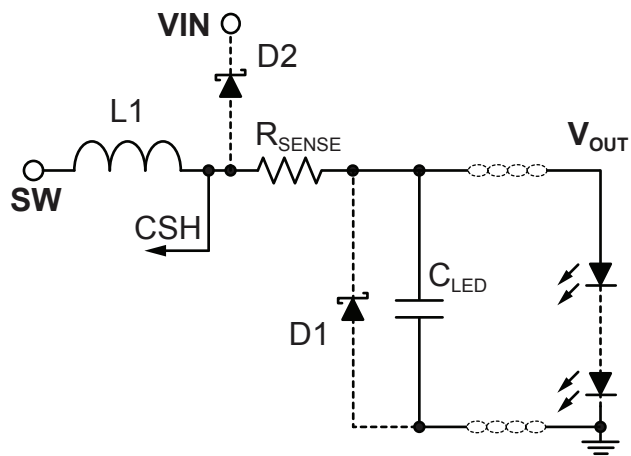
Figure 14: Clamp Diode D1 for LED Short Protection when V_{IN} is above 40 V. Clamp Diode D2 for LED Open Protection when V_{IN} is above 45 V.

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COMPONENT SELECTIONS

The inductor is often the most critical component in a buck converter. Follow the procedure below to derive the correct parameters for the inductor:

1. Determine the saturation current of the inductor. This can be done by simply adding 20% to the average LED current:

$$i_{SAT} \geq i_{LED} \times 1.2.$$

2. Determine the ripple current amplitude (peak-to-peak value). As a general rule, ripple current should be kept between 10% and 30% of the average LED current:

$$0.1 < i_{RIPPLE(pk\text{-}pk)} / i_{LED} < 0.3.$$

3. Calculate the inductance based on the following equations:

$$L = (V_{IN} - V_{OUT}) \times D \times t / i_{RIPPLE} \text{ , and}$$

$$D = V_{OUT} / V_{IN} \text{ ,}$$

where

   D is the duty cycle, and
   t is the period $1/f_{SW}$.

OUTPUT FILTER CAPACITOR

The ALT80800 is designed to operate in current regulation mode. Therefore it does not require a large output capacitor to stabilize the output voltage. This results in lower cost and smaller PCB area. In fact, having a large output capacitor is not recommended.

In most applications, however, it is beneficial to add a small filter capacitor (around 0.1 µF) across the LED string. This capacitor serves as a filter to eliminate switching spikes seen by the LED string. This is very important in reducing EMI noises, and may also help in ESD testing.

ADDITIONAL NOTES ON RIPPLE CURRENT

• For consistent switching frequency, it is recommended to choose the inductor and switching frequency to ensure the inductor ripple current percentage is at least 10% over normal operating voltage range (ripple current is lowest at lowest V_{IN}).

• If ripple current is less than 10%, the switching frequency may jitter due to insufficient ripple voltage across CSH and CSL pins. However, the average LED current is still regulated.

• For best accuracy in LED current regulation, a low current ripple of less than 20% is required.

• There is no hard limit on the highest ripple current percentage allowed. A 40% ripple current is still acceptable, as long as both the inductor and LEDs can handle the peak current (average current × 1.2 in this case). However, higher ripple current percentage affects the accuracy of LED current, and limits the minimum current that can be regulated when using ADIM.

• In general, allowing a higher ripple current percentage enables lower-inductance inductors to be used, which results in smaller size and lower cost.

• If lower ripple current is required for the LED string, one solution is to add a small capacitor (such as 1 to 2.2 µF) across the LED string from LED+ to ground. In this case, the inductor ripple current remains high while the LED ripple current is greatly reduced.

• The effectiveness of this filter capacitor depends on many factors, such as: switching frequency, inductors used, PCB layout, LED voltage and current, and so forth.

• The addition of this capacitor introduces a longer delay in LED current during PWM dimming operation. Therefore the accuracy of average LED current is reduced at short PWM on-time.

INDUCTOR SELECTION CHART

The chart in the figure below summarizes the relationship between LED current, switching frequency, and inductor value. Based on this chart: assuming LED current = 1 A and L = 22 µH, then minimum f_{SW} = 0.68 MHz in order to keep the ripple current at 20% or lower. If the switching frequency is lower, then a larger inductance must be used to meet the same ripple current requirement.
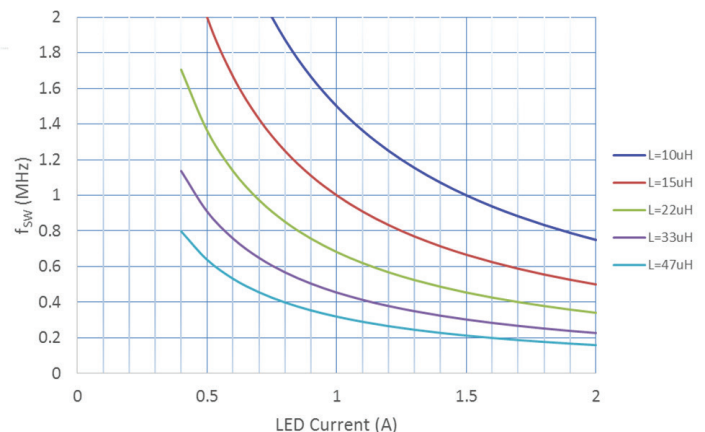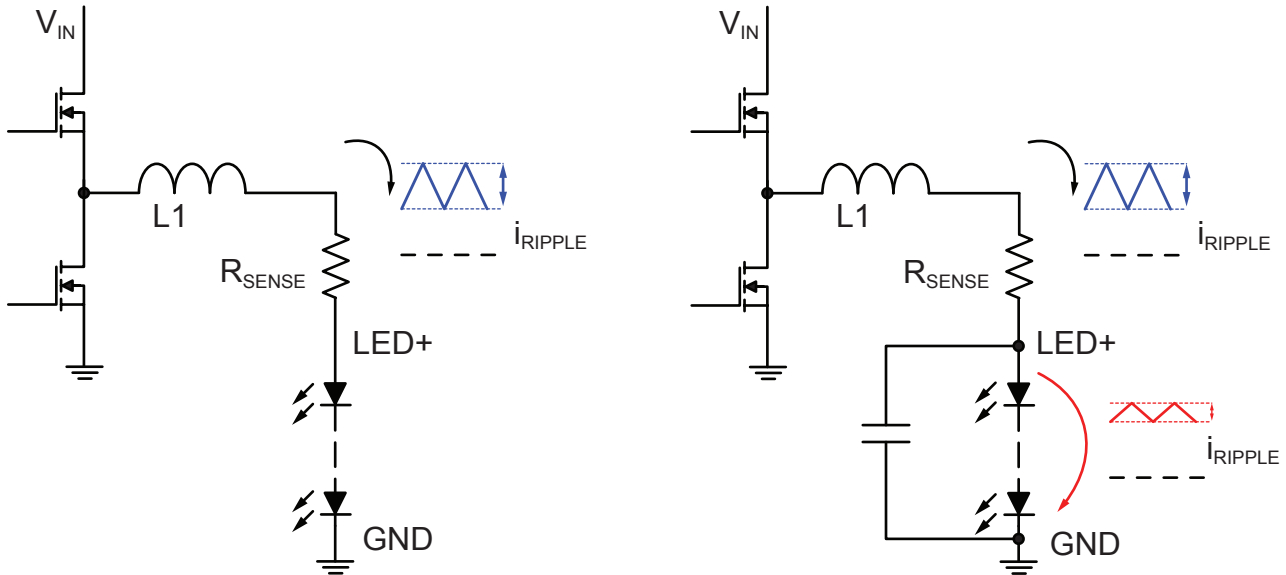

Figure 15: Minimum switching frequency vs. LED current, given different inductance used
(V_{IN} = 12 V, V_{OUT} = 6 V, ripple current = 20%)

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Effects of Output Capacitor on LED Ripple Current

Without output capacitor:
The same inductor ripple current flows through sense resistor and LED string.

With a small capacitor across LED string:
Ripple current through LED string is reduced, while ripple voltage across R_{SENSE} remains high.

**Figure 16: Using an Output Filter Capacitor to Reduce
Ripple Current in LED String**

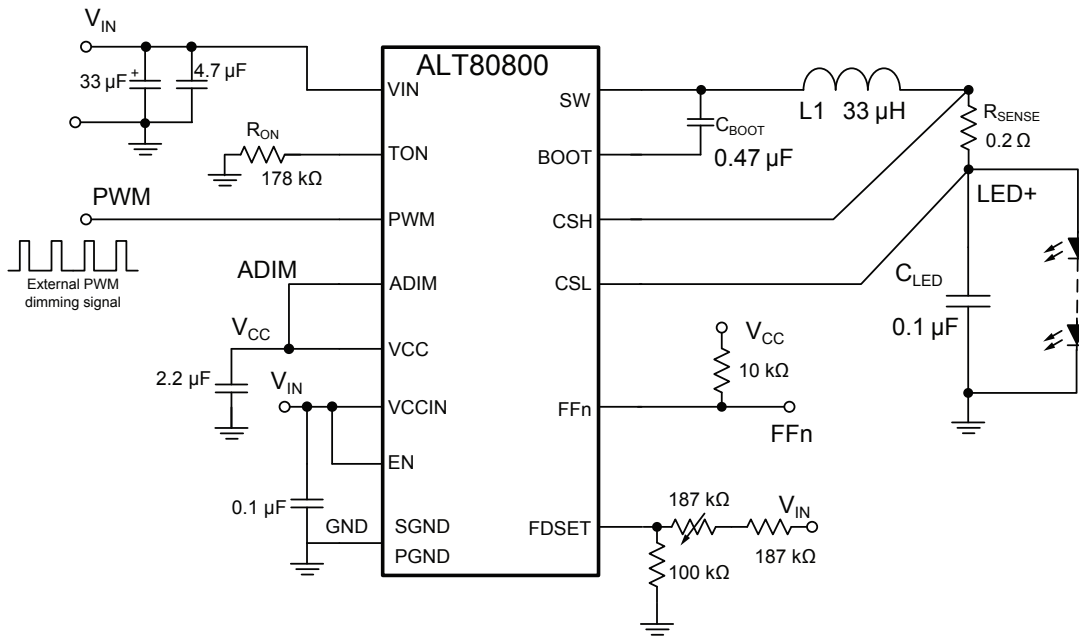## APPLICATION CIRCUIT DIAGRAMS

Figure 17: Application Circuit Example for ALT80800
(LED current = 1 A, 500 kHz)

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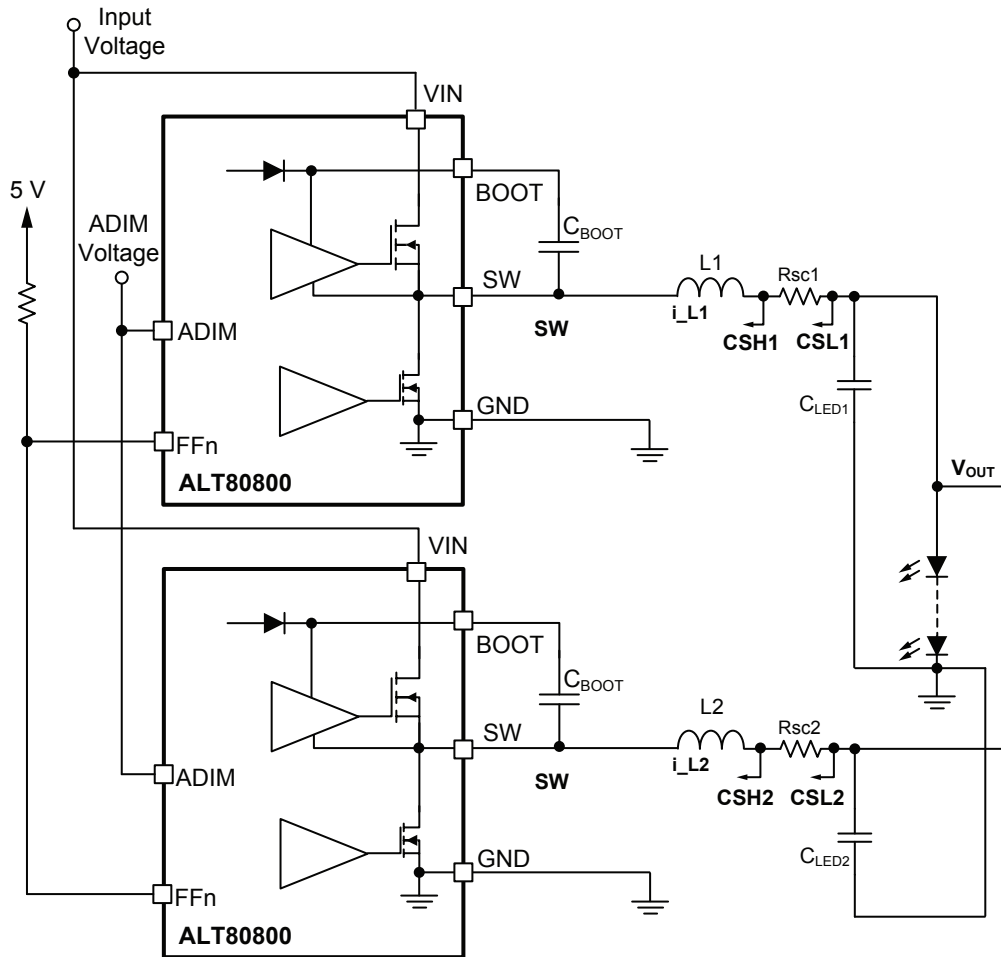
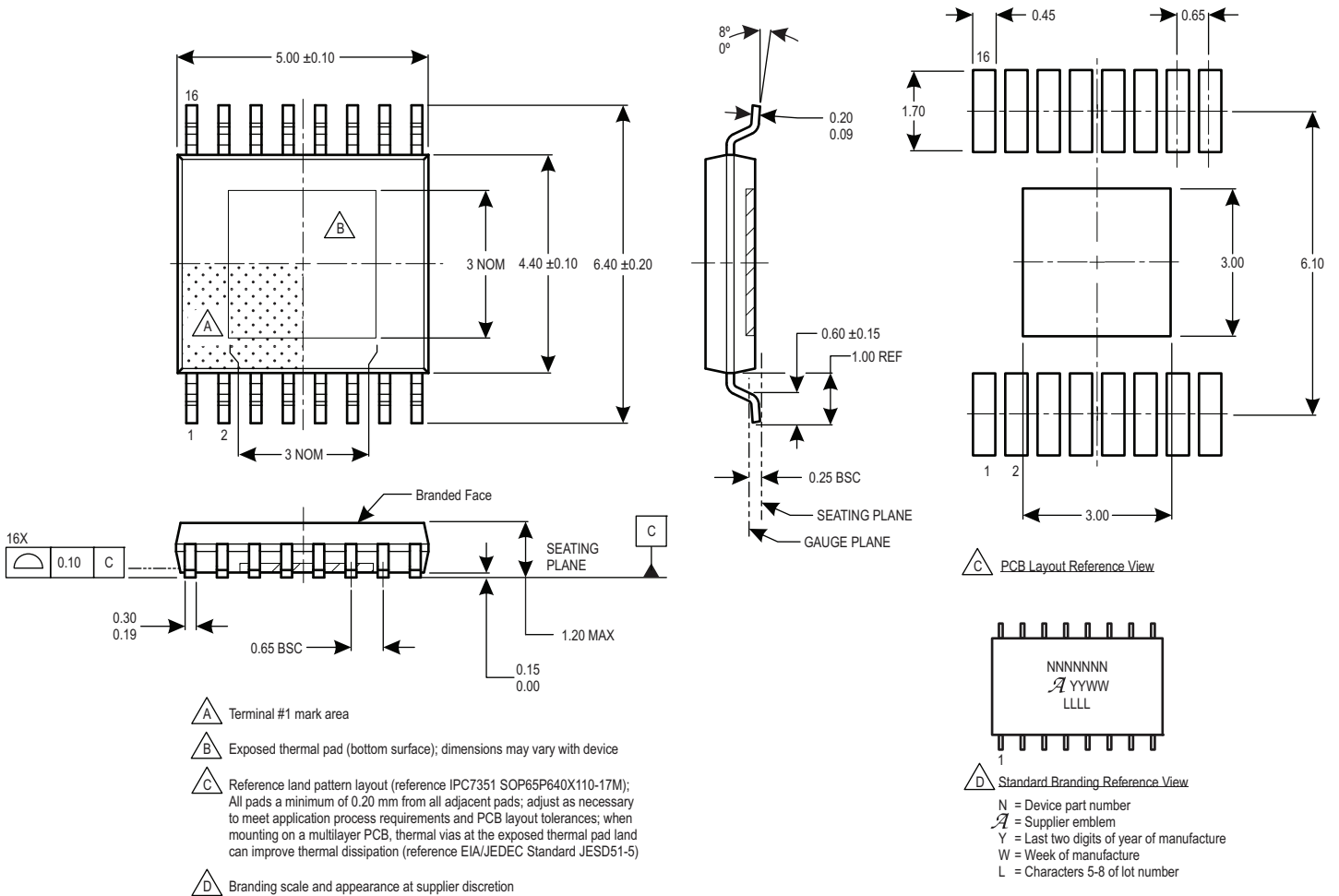19

APPLICATION CIRCUIT DIAGRAMS (continued)

**Figure 18: Using 2 (or more) ALT80800 in parallel to drive the same LED string.
Total LED current is the sum of currents from each LED driver.
(Note: each LED driver shares the same VIN and ADIM as illustrated).**

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use
(Reference MO-153 ABT)
Dimensions in millimeters. NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

8°
0°

0.20
0.09

5.00 ±0.10

16

B

3 NOM   4.40 ±0.10   6.40 ±0.20

A

1 2

3 NOM

0.60 ±0.15
1.00 REF

0.25 BSC

SEATING PLANE
GAUGE PLANE

0.45   0.65

16

1.70

1 2

3.00

3.00

6.10

C PCB Layout Reference View

Branded Face

16X

0.10 C

SEATING PLANE

C

0.30
0.19

0.65 BSC

1.20 MAX

0.15
0.00

NNNNNNN
A YYWW
LLLL

1

D Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Characters 5-8 of lot number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
to meet application process requirements and PCB layout tolerances; when
mounting on a multilayer PCB, thermal vias at the exposed thermal pad land
can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

Package LP, 16-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	December 7, 2017	Initial release

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