7-Output Stratum 3/3E SETS, G.8262 EEC Option 1 and 2, IEEE 1588 Network Synchronizer

```
Overview
========
Part:        Si5348
Design ID:   5348BP2
Created By:  ClockBuilder Pro v1.7 [2015-03-26]
Timestamp:   2015-03-26 09:25:11 GMT-05:00

Device Grade
============

Device       Output Clock
Grade        Frequency Range      Typical Jitter
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Si5348A*     100 Hz to 710.4 MHz  < 150 fs
Si5348B      100 Hz to 350 MHz    "

* Device Grade

Design
======
Host Interface:
    I/O Power Supply: VDD (Core)
    SPI Mode: 4-Wire
    I2C Address Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins)

XA/XB:
    48 MHz (XTAL - Crystal)

Inputs:
    IN0: Unused
    IN1: Unused
    IN2: Unused
    IN3: Unused
    IN4: Unused

Outputs:
    OUT0: Unused
    OUT1: Unused
    OUT2: Unused
    OUT3: Unused
    OUT4: Unused
    OUT5: Unused
    OUT6: Unused

Frequency Plan
==============
No plan
```

This datasheet addendum is provided as supplemental information to the Si5348A datasheet, located at www.silabs.com/timing. You can search for and download any datasheet addendum for Si534x/8x part numbers. Go to http://www.silabs.com/custom-timing for more information.

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