LOW-POWER 9-BIT INVERTER

SY100S321

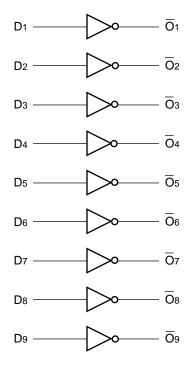
FEATURES

- Max. propagation delay of 700ps
- IEE min. of -55mA
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 70% faster than Fairchild 300K at lower power
- Internal 75k Ω input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output.

BLOCK DIAGRAM

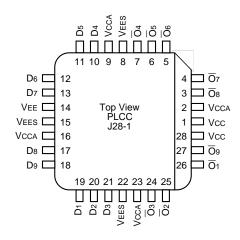


PIN NAMES

Pin	Function					
D1 – D9	Data Inputs					
$\overline{\mathbf{Q}}_1 - \overline{\mathbf{Q}}_9$	Data Outputs					
VEES	VEE Substrate					
VCCA	Vcco for ECL Outputs					

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PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S321JC	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JCTR ⁽¹⁾	J28-1	Commercial	SY100S321JC	Sn-Pb
SY100S321JZ ⁽²⁾	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S321JZTR ^(1, 2)	J28-1	Commercial	SY100S321JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
Iн	Input HIGH Current	_	_	200	μΑ	VIN = VIH (Max.)
IEE	Power Supply Current	- 55	-41	-25	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

		TA = 0°C		TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay ⁽¹⁾ Data to Output	300	700	300	700	300	700	ps	
tTLH tTHL	Transition Time ⁽¹⁾ 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts, G-G	Skew, Gate-to-Gate	_	200	_	200	_	200	ps	

NOTE:

^{1.} Reference Figures 1 and 2

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TEST CIRCUITRY⁽¹⁾

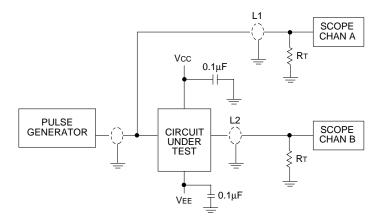


Figure 1. AC Test Circuit

Note:

1. VCC, VCCA = +2V, VEE = -2.5V.

L1 and L2 = equal length 50Ω impedance lines.

 $RT = 50\Omega$ terminator internal to scope.

Decoupling $0.1 \mu F$ from GND to Vcc and VEE.

All unused outputs are loaded with 50Ω to GND.

 C_L = Fixture and stray capacitance \leq 3pF.

SWITCHING WAVEFORMS

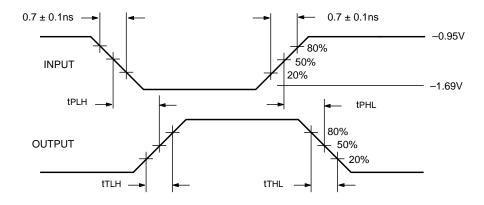


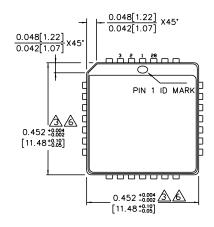
Figure 2. Propagation Delay and Transition Times

Note:

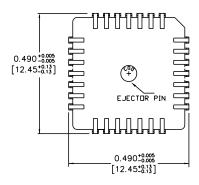
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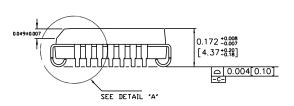
28-PIN PLCC (J28-1)



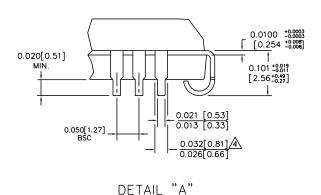
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Rev. A

NOTES:

DIMENSIONS ARE IN INCHES [MM].
CONTROLLING DIMENSION: INCHES.
DIMENSION DOES NOT INCLUDE MOLD FLASH
OR PROTRUSIONS, EITHER OF WHICH SHALL NOT
EXCEED 0.008 [0.203].
LEAD DIMENSION DOES NOT INCLUDE DAMBAR
PROTRUSION.

PROTRUSION.
MAXIMUM AND MINIMUM SPECIFICATIONS ARE
INDICATED AS FOLLOWS: MAX/MIN
PACKAGE TOP DIMENSION MAY BE SLIGHTLY
SMALLER THAN BOTTOM DIMENSION.

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