RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

This 79 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 716 to 960 MHz.

900 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1200 mA, P_{out} = 79 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
920 MHz	21.5	34.4	7.1	−34.6	−13
940 MHz	21.6	34.7	7.0	−33.5	−14
960 MHz	21.5	34.7	6.8	−33.6	−14

800 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1200 mA, P_{out} = 79 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.
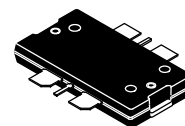
| Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
790 MHz	21.4	35.3	7.2	−35.1	−18
806 MHz	21.6	35.7	7.1	−34.5	−19
821 MHz	21.6	36.0	6.9	−34.3	−16

Features

- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications

A2T09VD300NR1

716–960 MHz, 79 W AVG., 48 V AIRFAST RF POWER LDMOS TRANSISTOR

TO-270WB-6A PLASTIC

RF$_{inA}$/V$_{GSA}$ 1   6 RF$_{outA}$/V$_{DSA}$
GND 2   5 GND
RF$_{inB}$/V$_{GSB}$ 3   4 RF$_{outB}$/V$_{DSB}$
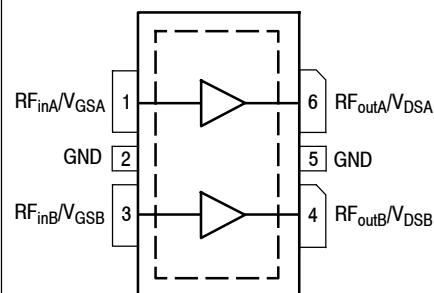
(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

freescale
Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	−0.5, +105	Vdc
Gate–Source Voltage	V_{GS}	−6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	−40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 98°C, 79 W CW, 48 Vdc, $I_{DQ(A+B)}$ = 1200 mA, 940 MHz	$R_{\theta JC}$	0.66	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	2
Machine Model (per EIA/JESD22–A115)	A
Charge Device Model (per JESD22–C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics [4]					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 116 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage (V_{DS} = 48 Vdc, $I_{DQ(A+B)}$ = 1200 mAdc)	$V_{GS(Q)}$	—	2.5	—	Vdc
Fixture Gate Quiescent Voltage [5] (V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1200 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.0	5.0	6.0	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.16 Adc)	$V_{DS(on)}$	0.1	0.21	0.5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf and search for AN1955.
4. Each side of device measured separately.
5. V_{GG} = 2 × $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistor divider network on the board. Refer to Test Fixture Layout.

A2T09VD300NR1

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In Freescale Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1200 mA, P_{out} = 79 W Avg., f = 920 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	20.0	21.5	23.0	dB
Drain Efficiency	η_D	31.5	34.4	—	%
Output Peak–to–Average Ratio @ 0.01% Probability on CCDF	PAR	6.6	7.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	−34.6	−32.0	dBc
Input Return Loss	IRL	—	−13	−10	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) $I_{DQ(A+B)}$ = 1200 mA, f = 940 MHz, 12 μsec(on), 10% Cycle					
VSWR 10:1 at 52 Vdc, 420 W Pulsed CW Output Power (3 dB Input Overdrive from 363 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, $I_{DQ(A+B)}$ = 1200 mA, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	250	—	W
P_{out} @ 3 dB Compression Point [3]	P3dB	—	398	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range)	Φ	—	−19	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	90	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 79 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (−30°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation over Temperature (−30°C to +85°C)	ΔP1dB	—	0.001	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T09VD300NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13–inch Reel	TO–270WB–6A

1. Part internally input matched.
2. Measurement made with device in single–ended configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W–CDMA single–carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
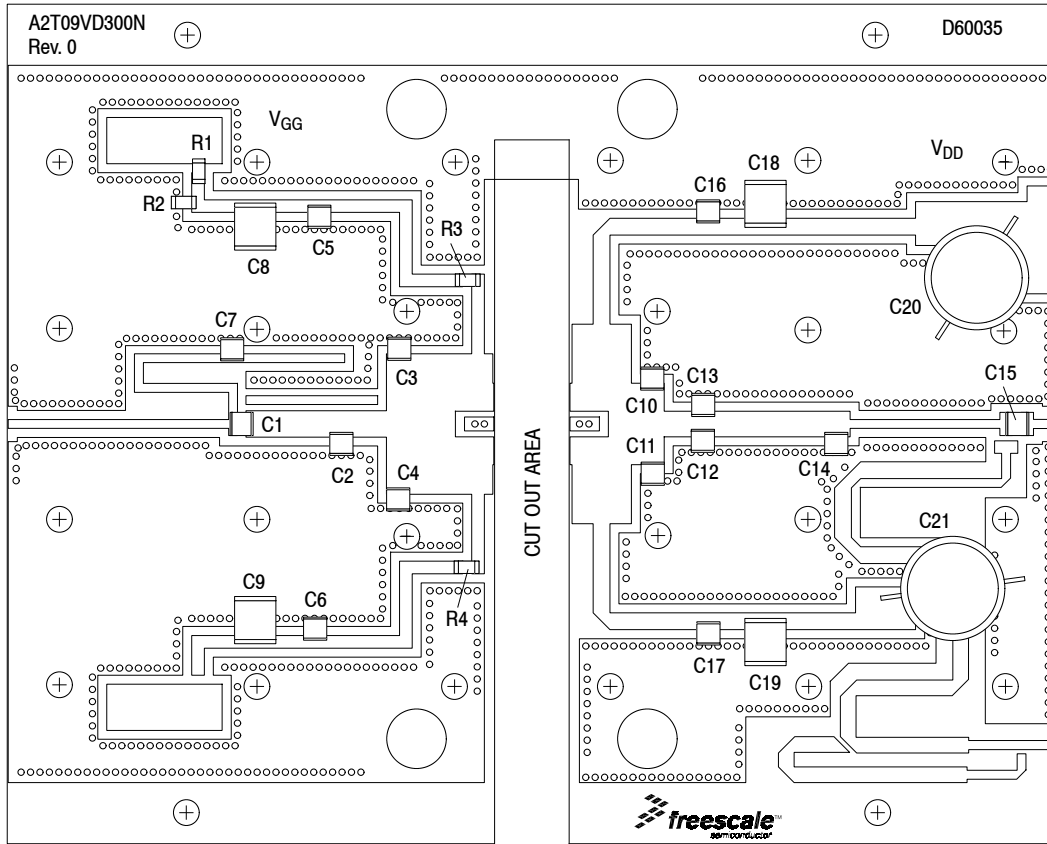
A2T09VD300NR1

Figure 2. A2T09VD300NR1 Test Circuit Component Layout

Table 7. A2T09VD300NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C3, C4	3.3 pF Chip Capacitors	ATC800B3R3BT500XT	ATC
C2	2.7 pF Chip Capacitor	ATC800B2R7BT500XT	ATC
C5, C6, C7, C15, C16, C17	47 pF Chip Capacitors	ATC800B470JT500XT	ATC
C8, C9	1 μF Chip Capacitors	C5750X7R2A105K230KM	TDK
C10, C11	15 pF Chip Capacitors	ATC800B150JT500XT	ATC
C12, C13	3 pF Chip Capacitors	ATC800B3R0BT500XT	ATC
C14	5.6 pF Chip Capacitor	ATC800B5R6BT500XT	ATC
C18, C19	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C20, C21	220 μF, 100 V Electrolytic Capacitors	MCGPR100V227M16X26–RH	Multicomp
R1, R2	1000 Ω, 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
R3, R4	10 Ω, 1/4 W Chip Resistors	CRCW120610R0JNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D60035	MTL

A2T09VD300NR1
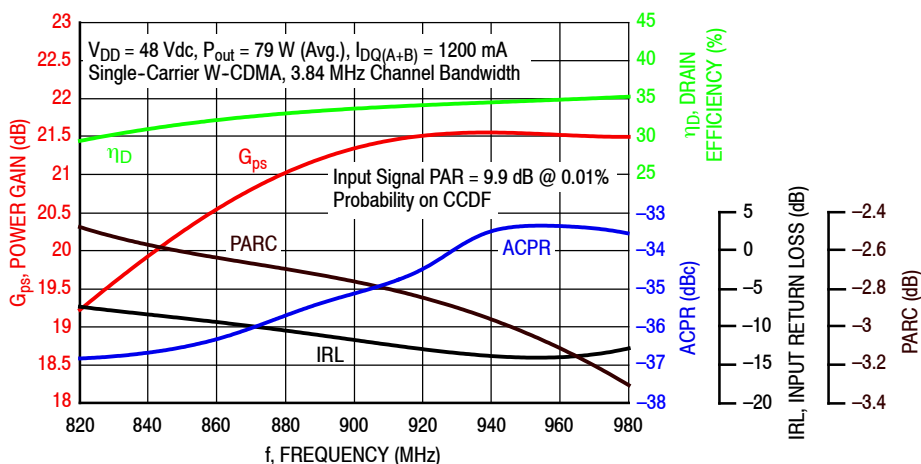
Figure 3. Single–Carrier Output Peak–to–Average Ratio Compression (PARC) Broadband Performance @ P_out = 79 Watts Avg.
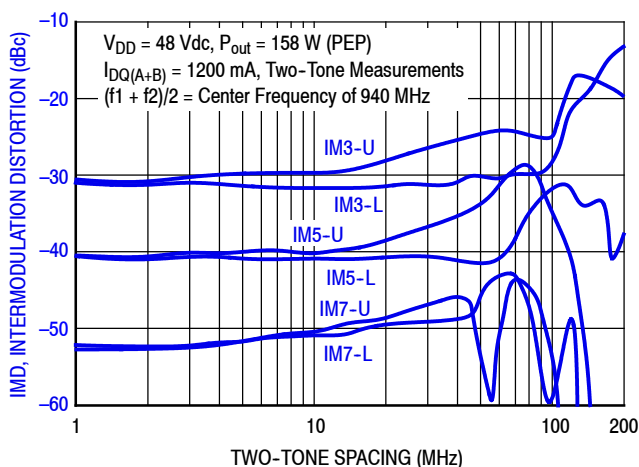
Figure 4. Intermodulation Distortion Products versus Two–Tone Spacing
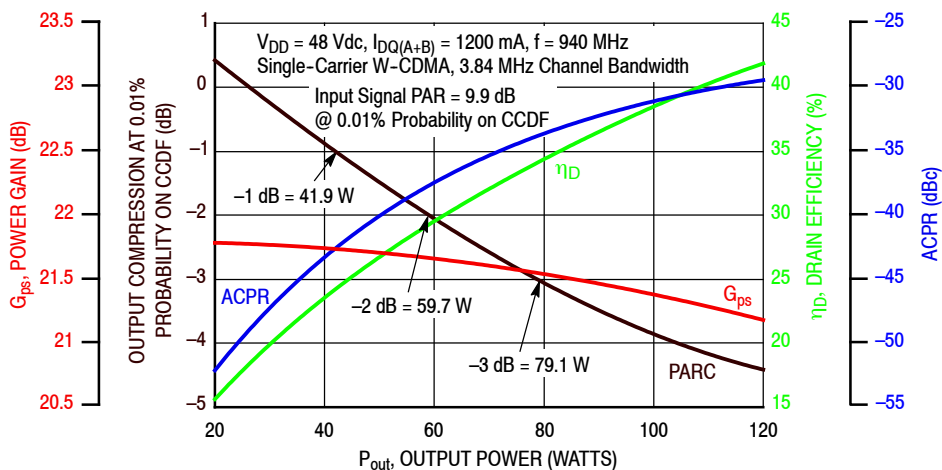
Figure 5. Output Peak–to–Average Ratio Compression (PARC) versus Output Power

A2T09VD300NR1

TYPICAL CHARACTERISTICS
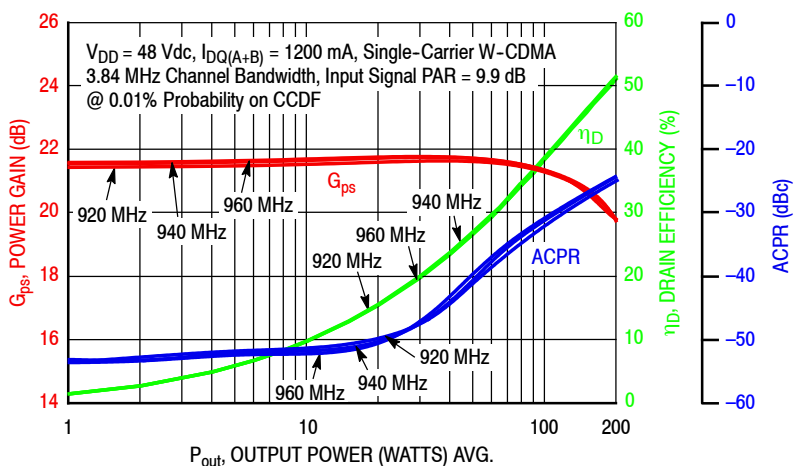
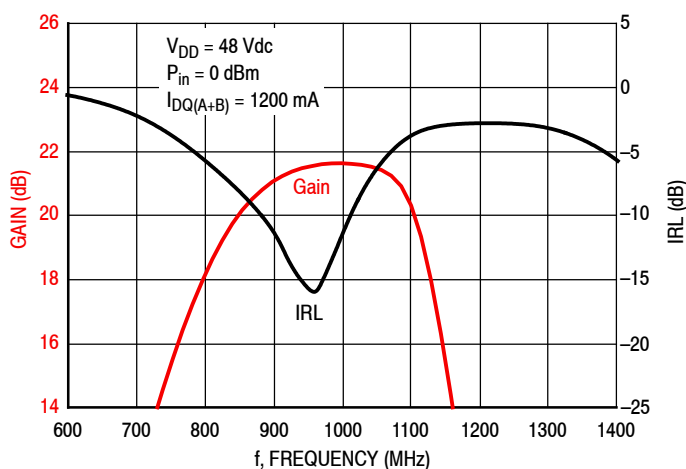**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**

Figure 7. Broadband Frequency Response

Table 8. Single Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 582 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} [1] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 − j4.77	2.79 + j5.52	2.53 + j0.15	20.3	53.1	202	60.0	−13
940	2.87 − j5.36	2.92 + j6.17	2.46 − j0.13	20.3	53.1	202	60.3	−12
960	3.52 − j5.36	2.87 + j6.65	2.24 − j0.21	20.3	53.0	200	60.3	−11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} [2] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 − j4.77	2.58 + j5.79	2.76 − j0.03	18.1	53.8	239	61.3	−18
940	2.87 − j5.36	2.68 + j6.48	2.68 − j0.25	18.2	53.8	238	61.5	−17
960	3.52 − j5.36	2.65 + j7.01	2.60 − j0.48	18.1	53.7	236	60.8	−16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Single Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 582 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} [1] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 − j4.77	2.43 + j5.57	1.96 + j2.30	22.7	50.9	124	70.1	−18
940	2.87 − j5.36	2.56 + j6.19	1.89 + j2.08	22.8	50.8	121	70.8	−18
960	3.52 − j5.36	2.55 + j6.68	1.83 + j1.71	22.4	51.0	125	70.2	−16

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} [2] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.52 − j4.77	2.37 + j5.85	2.31 + j1.99	20.3	52.3	170	71.6	−25
940	2.87 − j5.36	2.45 + j6.49	2.15 + j1.71	20.3	52.2	167	71.5	−25
960	3.52 − j5.36	2.42 + j7.01	2.02 + j1.46	20.2	52.2	165	71.2	−24

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Input Load Pull Tuner and Test Circuit → Z_{source} Z_{in} → Device Under Test → Z_{load} → Output Load Pull Tuner and Test Circuit

A2T09VD300NR1
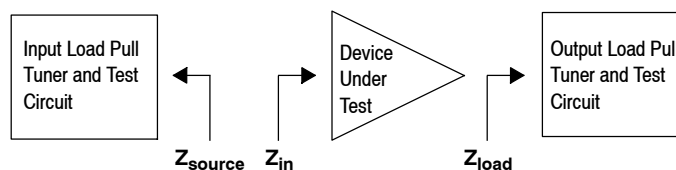
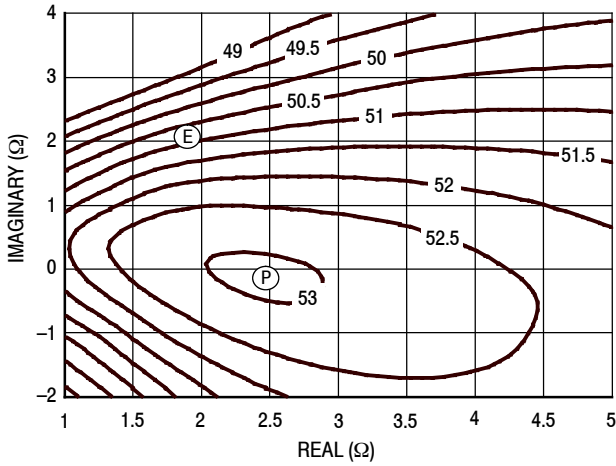## P1dB – TYPICAL LOAD PULL CONTOURS — 940 MHz

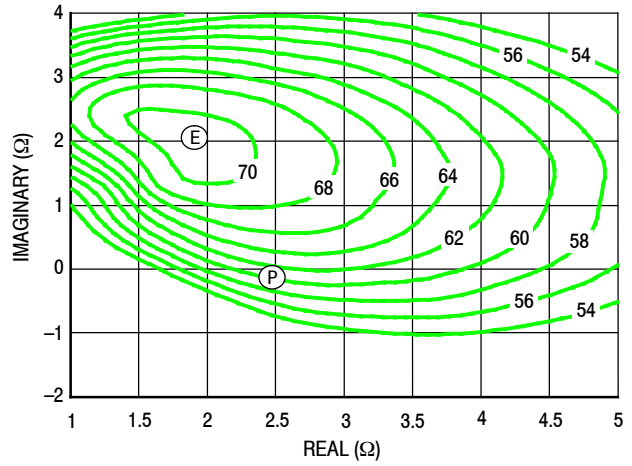**Figure 8. P1dB Load Pull Output Power Contours (dBm)**

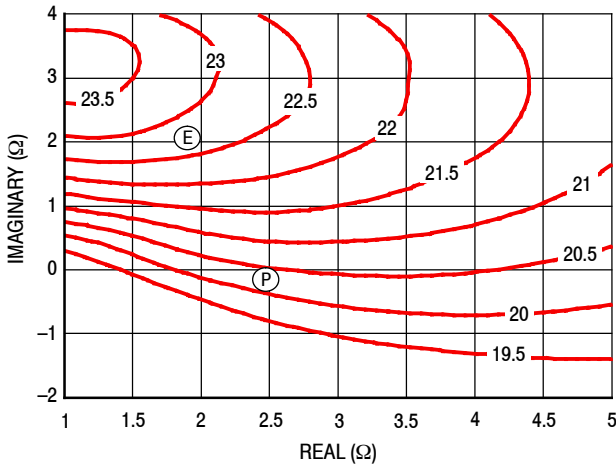**Figure 9. P1dB Load Pull Efficiency Contours (%)**
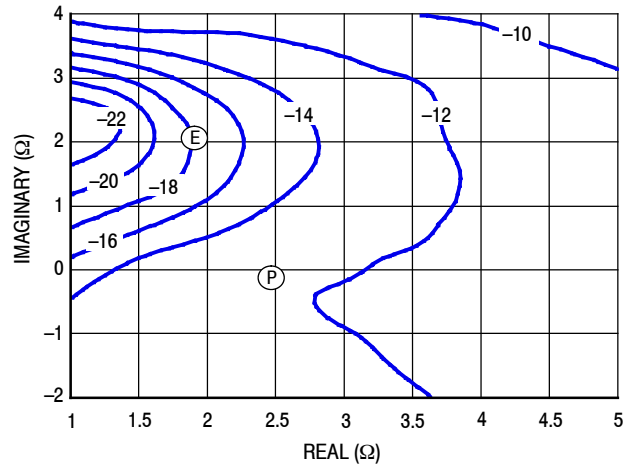

Figure 10. P1dB Load Pull Gain Contours (dB)

Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

— Gain
— Drain Efficiency
— Linearity
— Output Power

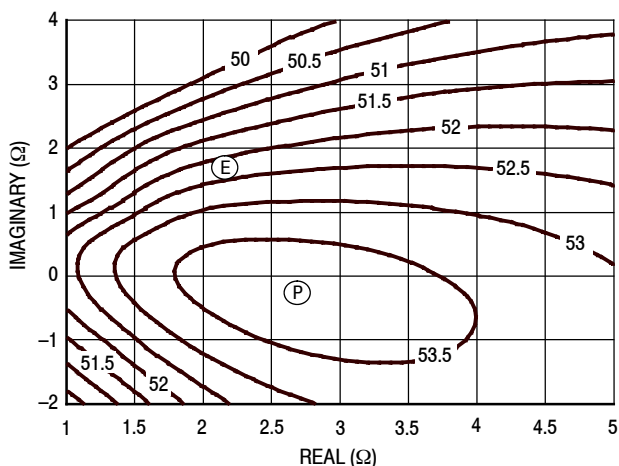## P3dB – TYPICAL LOAD PULL CONTOURS — 940 MHz
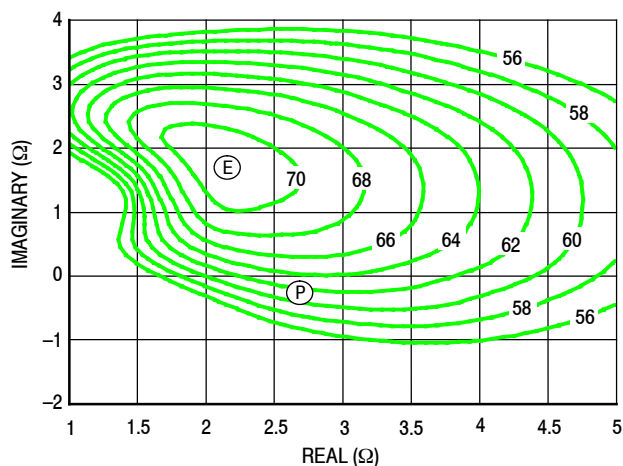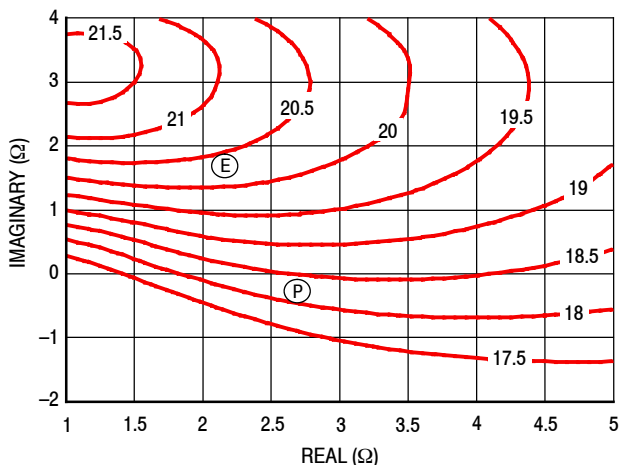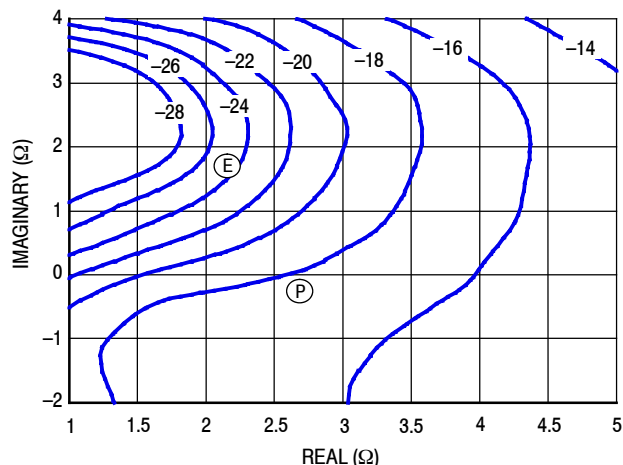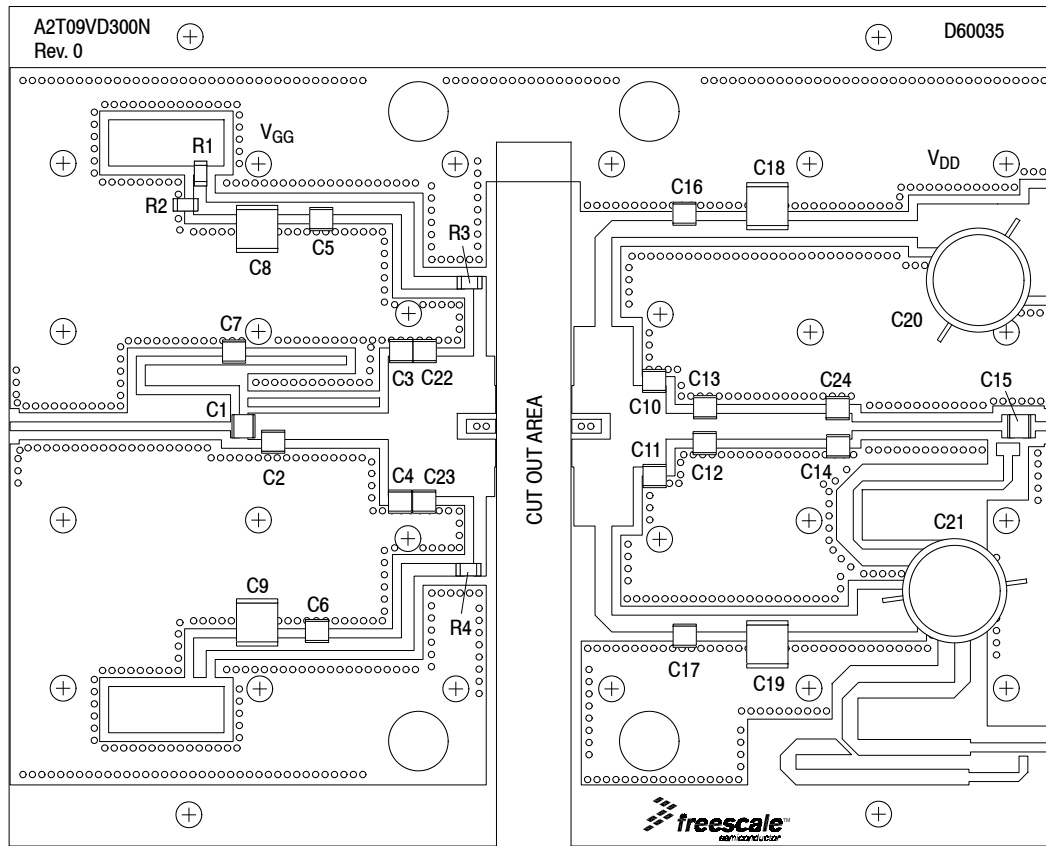

Figure 12. P3dB Load Pull Output Power Contours (dBm)

Figure 13. P3dB Load Pull Efficiency Contours (%)

Figure 14. P3dB Load Pull Gain Contours (dB)

Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

— Gain
— Drain Efficiency
— Linearity
— Output Power

A2T09VD300NR1

Figure 16. A2T09VD300NR1 Test Circuit Component Layout — 790–821 MHz

Table 10. A2T09VD300NR1 Test Circuit Component Designations and Values — 790–821 MHz

| Part	Description	Part Number	Manufacturer
C1, C3, C4, C22, C23	3.3 pF Chip Capacitors	ATC800B3R3BT500XT	ATC
C2	3.9 pF Chip Capacitor	ATC800B3R9BT500XT	ATC
C5, C6, C7, C15, C16, C17	47 pF Chip Capacitors	ATC800B470JT500XT	ATC
C8, C9	1 µF Chip Capacitors	C5750X7R2A105K230KM	TDK
C10, C11	18 pF Chip Capacitors	ATC800B180JT500XT	ATC
C12, C13	3.6 pF Chip Capacitors	ATC800B3R6BT500XT	ATC
C14	6.8 pF Chip Capacitor	ATC800B6R8BT500XT	ATC
C18, C19	10 µF Chip Capacitors	C5750X7S2A106M230KB	TDK
C20, C21	220 µF, 100 V Electrolytic Capacitors	MCGPR100V227M16X26–RH	Multicomp
C24	0.5 pF Chip Capacitor	ATC800B0R5BT500XT	ATC
R1, R2	1000 Ω, 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
R3, R4	10 Ω, 1/4 W Chip Resistors	CRCW120610R0JNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D60035	MTL

A2T09VD300NR1
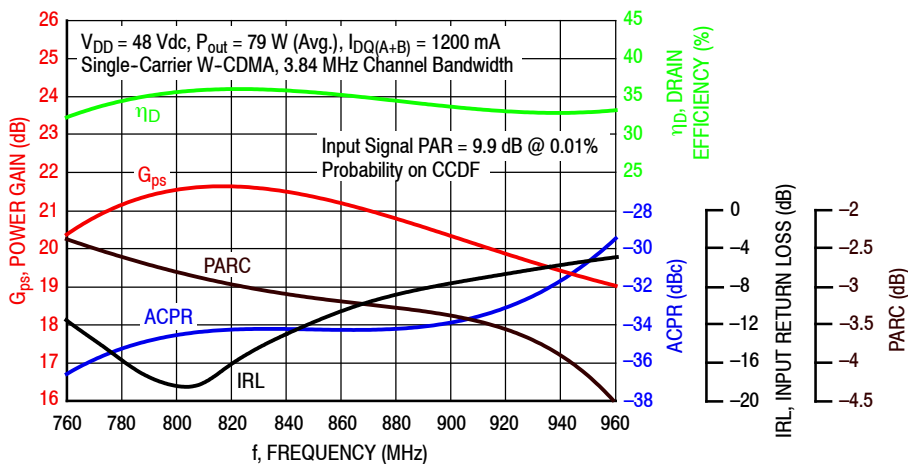
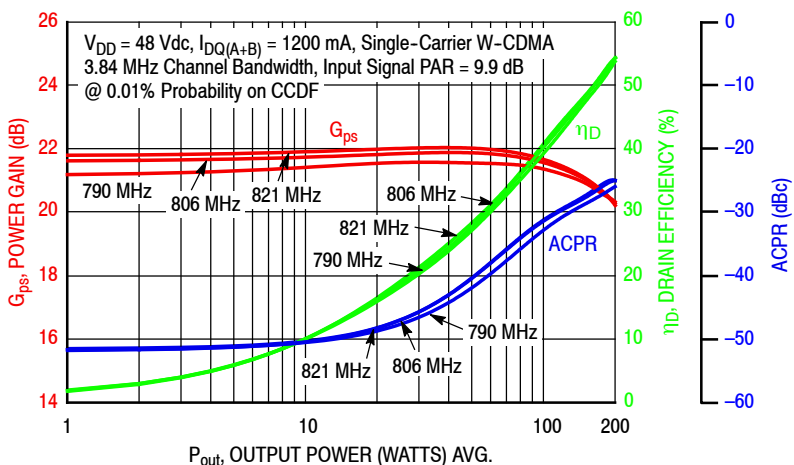**Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_out = 79 Watts Avg.**

Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power
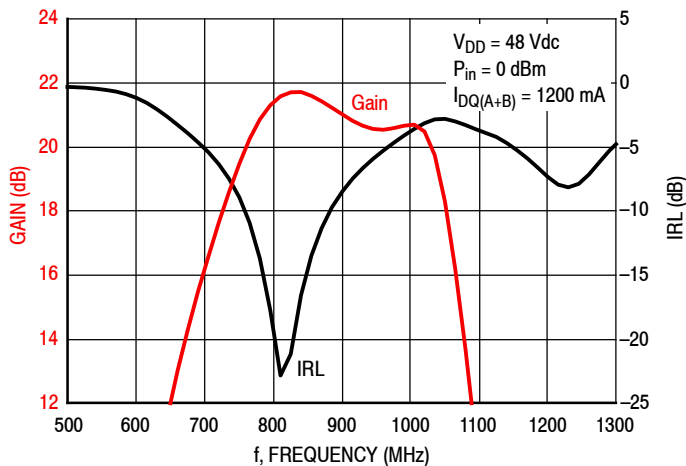

Figure 19. Broadband Frequency Response

A2T09VD300NR1

Table 11. Single Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQ} = 588 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} [1] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.02 − j2.72	2.66 + j3.14	2.84 + j1.14	19.9	53.5	223	63.7	−10
806	3.29 − j2.85	2.58 + j3.43	2.70 + j1.24	20.1	53.4	218	62.9	−11
821	3.26 − j3.34	2.47 + j3.75	2.65 + j1.27	20.3	53.3	215	63.3	−11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} [2] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.02 − j2.72	2.48 + j3.26	2.94 + j1.04	17.9	54.1	259	65.9	−14
806	3.29 − j2.85	2.42 + j3.58	2.99 + j1.01	18.0	54.1	255	64.8	−14
821	3.26 − j3.34	2.31 + j3.89	2.82 + j0.99	18.0	54.0	253	64.3	−14

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 12. Single Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQ} = 588 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} [1] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.02 − j2.72	2.12 + j3.24	2.51 + j4.27	22.9	50.6	115	76.2	−17
806	3.29 − j2.85	2.22 + j3.55	2.82 + j3.70	22.4	51.5	141	74.7	−15
821	3.26 − j3.34	2.19 + j3.86	2.83 + j3.42	22.3	51.7	148	74.1	−15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} [2] (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
790	3.02 − j2.72	2.29 + j3.37	3.54 + j3.22	19.7	52.8	189	74.2	−18
806	3.29 − j2.85	2.14 + j3.73	3.06 + j3.78	20.3	52.1	164	74.5	−20
821	3.26 − j3.34	2.07 + j4.04	2.96 + j3.63	20.4	52.2	165	74.8	−21

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Input Load Pull Tuner and Test Circuit — Device Under Test — Output Load Pull Tuner and Test Circuit

Z_{source} Z_{in} Z_{load}
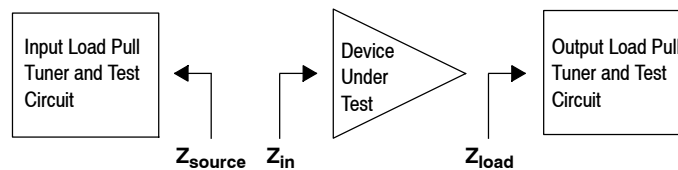
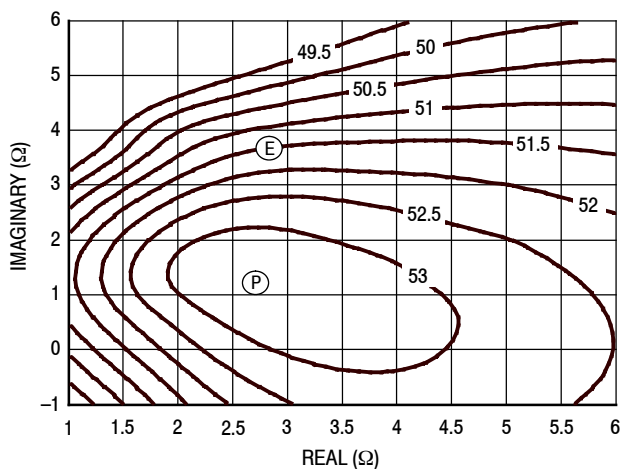## P1dB – TYPICAL LOAD PULL CONTOURS — 806 MHz

Figure 20. P1dB Load Pull Output Power Contours (dBm)
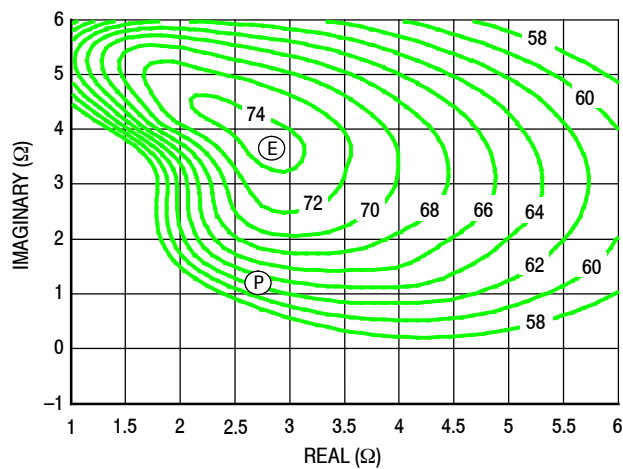

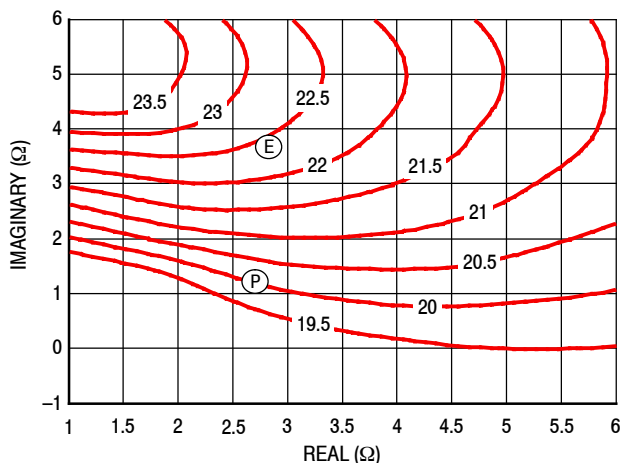Figure 21. P1dB Load Pull Efficiency Contours (%)
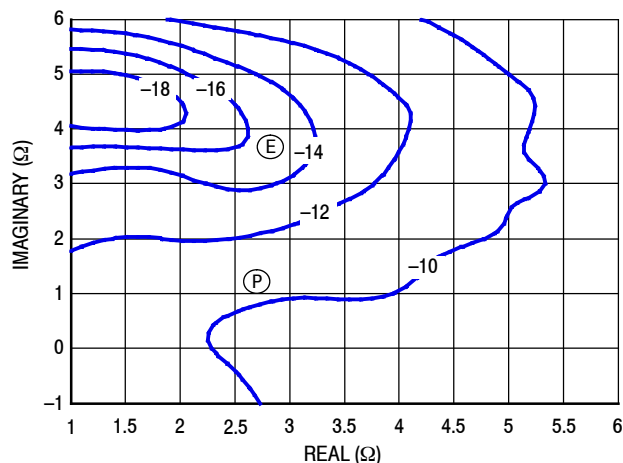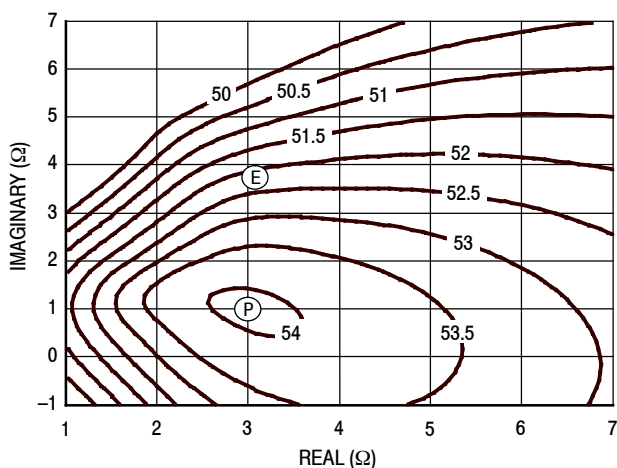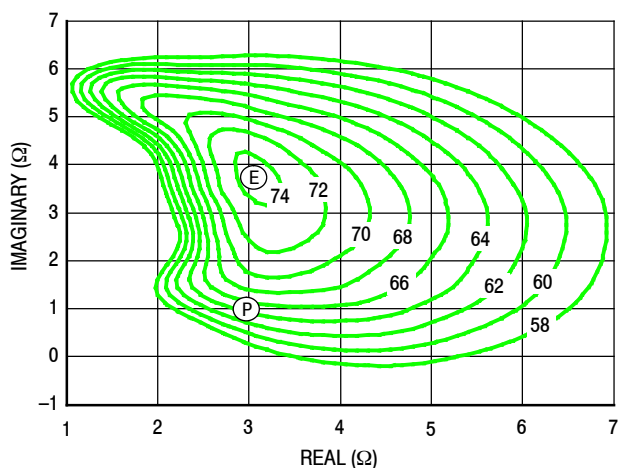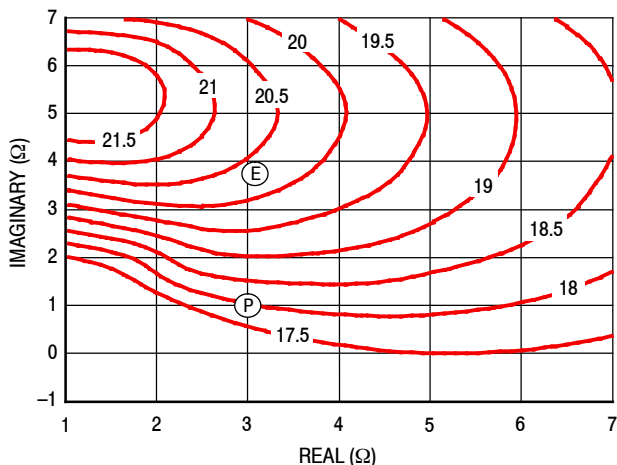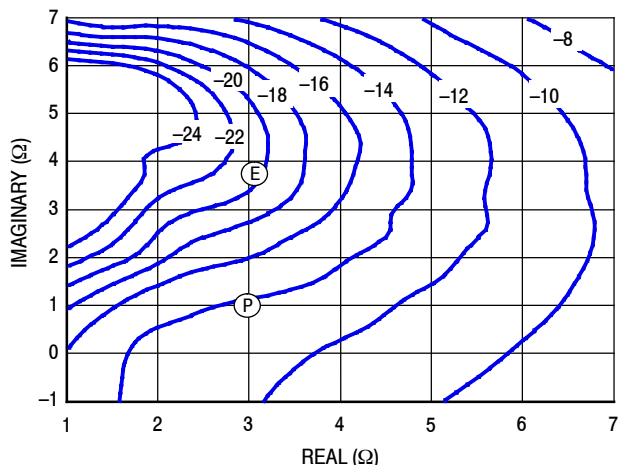

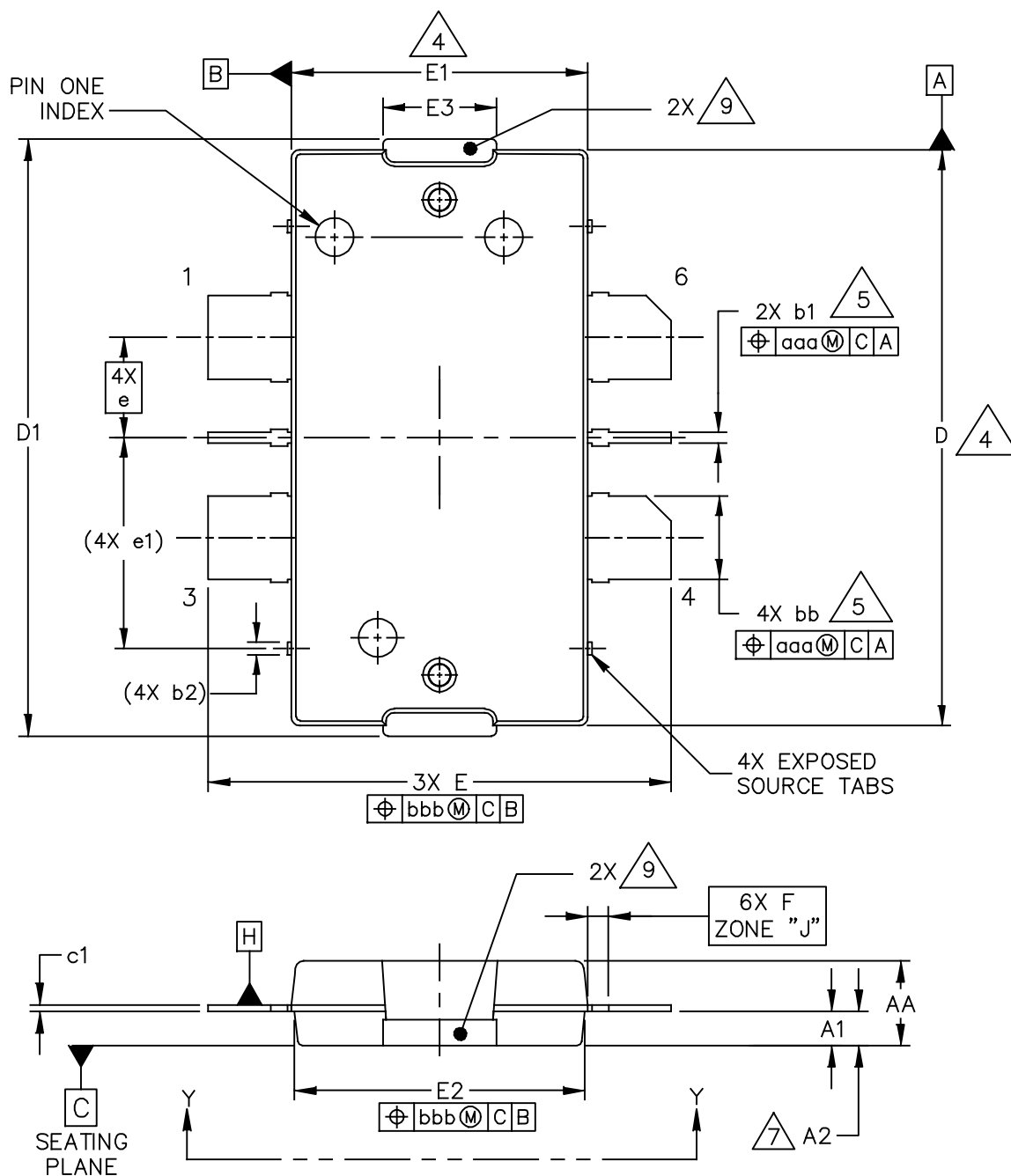Figure 22. P1dB Load Pull Gain Contours (dB)

Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

—— Gain
—— Drain Efficiency
—— Linearity
—— Output Power

A2T09VD300NR1

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 806 MHz

Figure 24. P3dB Load Pull Output Power Contours (dBm)

Figure 25. P3dB Load Pull Efficiency Contours (%)

Figure 26. P3dB Load Pull Gain Contours (dB)

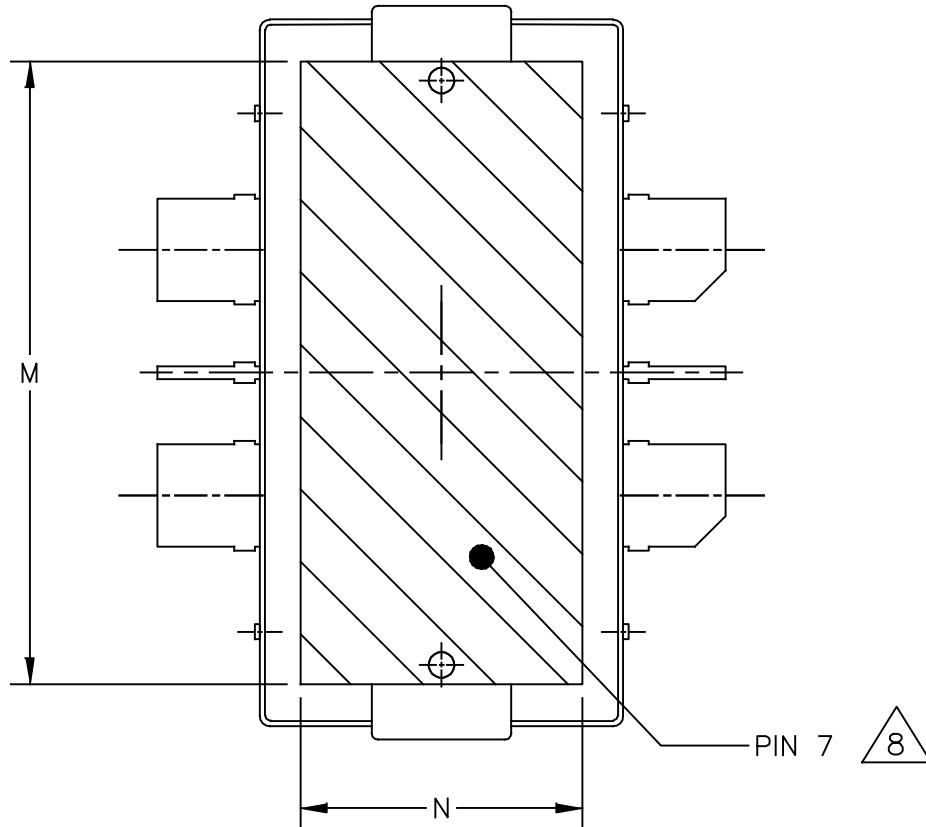Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

—— Gain
—— Drain Efficiency
—— Linearity
—— Output Power

PACKAGE DIMENSIONS

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VIEW Y—Y

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NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.099	.105	2.51	2.67	M	.600	———	15.24	———
A1	.039	.043	0.99	1.09	N	.270	———	6.86	———
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	b2	———	.019	———	0.48
E	.551	.559	14.00	14.20	c1	.007	.011	0.18	0.28
E1	.353	.357	8.97	9.07	e	.120 BSC		3.05 BSC	
E2	.346	.350	8.79	8.89	e1	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	aaa	.004		0.10	
F	.025 BSC		0.64 BSC		bbb	.008		0.20	

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A2T09VD300NR1

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

• AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

• EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

• Electromigration MTTF Calculator
• RF High Power Model
• s2p File

Development Tools

• Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.freescale.com/rf
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2015	• Initial Release of Data Sheet

A2T09VD300NR1

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