Technical Note

TN_175

FT4222H Revision D

Version 1.0

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The intention of this technical note is to give a detailed description of improvement available in the FT4222H Revision D device. The current revision of the FT4222H series is **Revision D, released April 2018.**

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1 Introduction

The FT4222H is a Hi-Speed USB interface device which supports SPI and I^2C communication protocol with configurable interfaces. The SPI interface can be configured in master mode with single, dual, or quad bits data width transfer or in slave mode with single bit data width transfer.

The modification and improvement in rev D of the FT4222H is described as below sections.

1.1 Buffer Size for Data Stream is changed in CNFMODE1 and CNFMODE2

In CNFMODE1 and CNFMODE2, 4 USB interfaces are enabled. In FT4222H Rev D, the buffer operation for IN and OUT pipes is changed to a 512 bytes single buffer instead of 256 bytes dual banks to match the maximum packet size defined for a bulk transfer in a USB high-speed device. In CNFMODE0, the buffer operation for GPIOs is also changed to 512 bytes double buffers.

Max. Packet Size and No. of Buffer Bank	FT4222H Rev D			
	CNFMODE0	**CNFMODE1**	**CNFMODE2**	**CNFMODE3**
Interface A	Data Stream 512 Bytes Dual Banks	Data Stream 512 Bytes Single Bank	Data Stream 512 Bytes Single Bank	Data Stream 512 Bytes Dual Banks
Interface B	For GPIOs 512 Bytes Dual Banks	Data Stream 512 Bytes Single Bank	Data Stream 512 Bytes Single Bank	Disable
Interface C	Disable	Data Stream 512 Bytes Single Bank	Data Stream 512 Bytes Single Bank	Disable
Interface D	Disable	For GPIOs 512 Bytes Single Bank	Data Stream 512 Bytes Single Bank	Disable

Table 1 Endpoint Maximum Packet Size and Buffer Configuration in Rev D

Max. Packet Size and No. of Buffer Bank	FT4222H Rev A/B/C			
	CNFMODE0	**CNFMODE1**	**CNFMODE2**	**CNFMODE3**
Interface A	Data Stream 512 Bytes Dual Banks	Data Stream 256 Bytes Dual Bank	Data Stream 256 Bytes Dual Bank	512 Bytes Dual Banks
Interface B	For GPIOs 8 Bytes Dual Banks	Data Stream 256 Bytes Dual Bank	Data Stream 256 Bytes Dual Bank	Disable
Interface C	Disable	Data Stream 256 Bytes Dual Bank	Data Stream 256 Bytes Dual Bank	Disable
Interface D	Disable	For GPIOs 8 Bytes Dual Banks	Data Stream 256 Bytes Dual Bank	Disable

Table 2 Endpoint Maximum Packet Size and Buffer Configuration in Rev A,B,C

The following table shows the maximum throughput that can be expected within each configuration mode. The calculations assume the FT4222H is operating with a high operating frequency on SCK and the USB bus has enumerated the device as a high speed with sufficient bandwidth. For example, the max throughput that can be expected is up to 52.8Mbps when the operating clock is equal to 80MHz, SCK is set as 40MHz, only 1 data stream interface is enabled not 3 or 4, the data bus is operating in quad mode and the USB bus is operating at hi-speed USB rates with sufficient bandwidth.

Throughput (Unit : Mbps)		FT4222H Rev D			
		CNFMODE0	**CNFMODE1**	**CNFMODE2**	**CNFMODE3**
QuadSPI Master	**Single Mode (1 bit)**	27.8 (Write/Read)	22.8 (Write/Read)	23.0 (Write/Read)	27.3 (Write/Read)
	Dual Mode (2 bit)	39.7(Write) 42.7(Read)	31.3(Write) 38.1(Read)	31.4(Write) 38.7(Read)	39.6(Write) 42.5(Read)
	Quad Mode (4 bit)	53.3(Write) 48.5(Read)	41.6(Write) 42.1(Read)	41.9(Write) 42.8(Read)	52.8(Write) 49.7(Read)

Table 3 Maximum throughput for QuadSPI Master Controller in Rev. D

1.2 USB-IF Test-ID

As a consequence of the modification described in Section 1.1, USB compliance for the FT4222H IC was re-tested and a new USB-IF Test-ID distributed in March 2018.

TID for FT4222H IC Rev D : 40001830
TID for FT4222H IC Rev A : 40001599

TID for UMFT4222EV with FT4222HQ-D : 10007740
TID for UMFT4222EV with FT4222HQ-A : 10007262

1.3 Improve the Detectable Frequency on GPIOs

Limitation before Rev-D

The maximum detectable frequency on GPIOs is 4KHz in the version before revision-D

Design Change in Rev-D

Add a higher detection mechanism to increase the detectable frequency on GPIOs. The following table shows the maximum frequency that can be detected on GPIOs. Note that this new higher detection function is disabled by default and can be enabled via APIs defined in LibFT4222.

Max. Freq. can be detected	**GPIO**			**GPIO3 as Interrupt input source**		
Operating clock Frequency	With operating SPI pipe	With operating I2C pipe	Only GPIO pipe operates	With operating SPI pipe	With operating I2C pipe	Only GPIO pipe operates
60MHz	< 10KHz	< 2KHz	< 20KHz	< 20KHz	< 4KHz	< 40KHz
80MHz	< 10KHz	< 4KHz	< 30KHz	< 60KHz	< 8KHz	< 70KHz

Table 4 Detectable Frequency on GPIOs

2 FT4222H Series Package Markings

The FT4222H is supplied in a RoHS compliant leadless VQFN-32 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC. An example of the markings on the package is shown in the figures below.

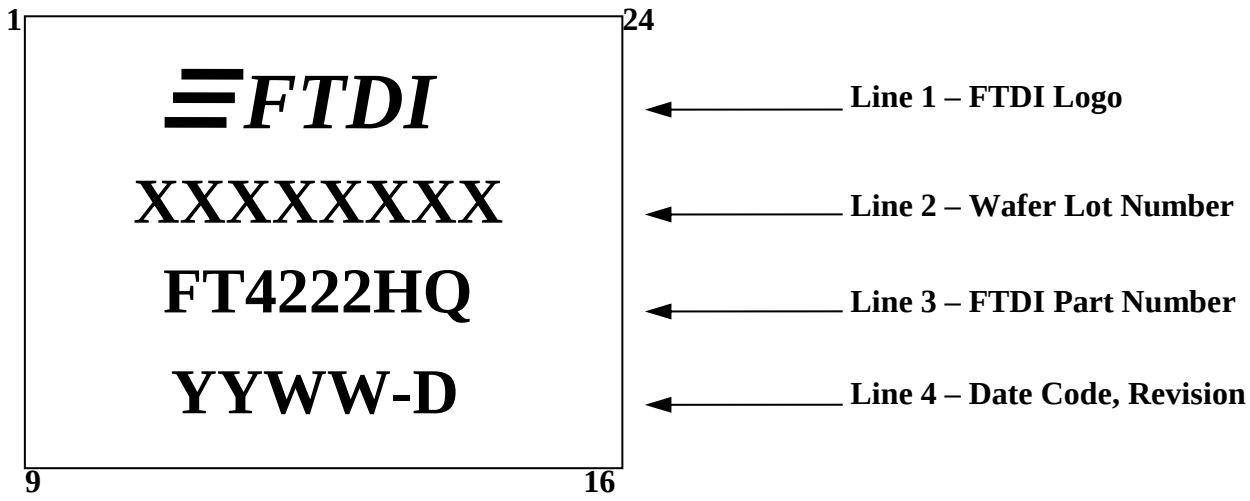

Figure 1 VQFN-32 Package Markings

The date code format is **YYWW** where WW = 2 digit week number, YY = 2 digit year number. This is followed by the revision number.

The code **XXXXXXXX** is the manufacturing LOT code

3 Contact Information

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Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country

Appendix A – References

Document References

DS_FT4222H

Acronyms and Abbreviations

Terms	Description
GPIO	General Purpose Input/output
I2C	Inter-Integrated Circuit
RoHS	Restriction of Hazardous Substances Directive
SCK	Serial Clock
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
VQFN	Very Thin Quad Flat Non-Leaded Package

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Appendix C – Revision History

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Product Page: http://www.ftdichip.com/Products/ICs/FT4222H.html
Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	2018-04-03