DARR83

Wireless Audio Processor with Tri-Band Support and Embedded Multi-Channel USB 2.0 Audio Controller

PRODUCT FEATURES

Data Brief

Highlights

- Single, dual and tri-band (2.4/5.2/5.8 GHz)
- 22 Mbps wireless air data rate
- Up to four uncompressed stereo audio channels
- Bi-directional audio support, allowing simultaneous RX and TX on a single device
- 16-24 bit, 44.1-96 kHz stereo audio transmission
- Integrated USB controller and PHY, offering wireless multi-channel audio
- Bi-directional data channel (up to 100 kbps)
- Point-to-point and point-to-multi-point support
- In-room range up to 50 m
- Video data transfer up to 10 Mbps
- Seamless RF band/channel switching
- Configurable, low latency audio, default at 18 ms
- Real-time Wi-Fi® sniffer
- Excellent Quality of Service (QoS)
- Low power consumption
- Single 3.3 V operation
- 129-pin, FBGA package

Target Applications

- Wireless subwoofers
- Wireless soundbars
- Fully wireless 5.1 and 7.1 home cinema applications
- Wireless headphones systems and headsets
- Wireless microphones
- Wireless USB audio dongles
- Automotive infotainment systems
- Digital televisions
- Set-top boxes
- Laptops
- Gaming systems
- Wireless home audio networks

Key Benefits

- High quality audio
  - Low latency of less than 20 ms, supporting wireless audio for video and gaming applications
  - Tight inter-speaker synchronization
  - Audio quality up to 24 bit, 96 kHz
  - Low latency compression algorithm, optimized for voice applications and headsets
- Wireless
  - Enhanced robustness against both in and out of band interferers, such as microwave ovens
  - Excellent coexistence with 802.11b/g/n Wi-Fi, cordless phones and Bluetooth®, even when collocated in the same device
  - Automatic receiver antenna diversity minimizing fading and multi-path effects
  - Link quality monitoring
  - Soft audio muting under poor link circumstances
  - Automatic TX output power control, minimizing RF footprint
- Networking and Connectivity
  - Supports multi-room network topologies
  - Bi-directional audio
  - Simple pairing and association functions
  - Control data communications between devices up to 100 kbps
  - Backwards compatible to all application modes of previous DARR generations including DARR80, 81 and 82
- Interfacing and Integration
  - Quad I²S™ or stereo S/PDIF input/output
  - Master and Slave I²C™ bus for external control functions
  - Integrated SRC and MCU
  - Integrated USB2.0 Controller and PHY, offering a bi-directional, multi channel USB audio interface
- Optimized pre-certified modules available[1]

1. For more information, refer to www.smsc.com or your local sales contact.

PRODUCT PREVIEW

Order Number(s):

DARR83 for 129-pin FBGA package, RoHS-compliant package

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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General Description

SMSC's DARR83 enables a wide range of digital wireless audio applications. It offers a high level of integration resulting in a very low-cost complete wireless system solution, without any sacrifice to the main technology drivers: Audio Quality and Wireless Fidelity.

From a high-level perspective the DARR83 consists of a number of function blocks, each connected through an internal parallel bus, see Figure 1. The core wireless audio functionality of the DARR83 is implemented in the following top function blocks:

- Audio
- Data Link
- PHY

The Audio function block forms the interface between on the left side the audio interfaces, such as S/PDIF and I^2S, and on the right side the audio buffers for the Data Link. The Audio function block takes care of all functions related to audio buffering, audio routing, audio integrity, sample clock synchronization, sample rate conversion and volume control.

The Data Link packs the data when transmitting the audio information into a data stream, directly suitable for modulation by the PHY. When receiving the data, the Data Link block performs the unpacking and verification of the wireless packets. The Data Link also takes care of the exact timing of all the wireless activities. Additionally, it performs the control data messaging.

The PHY performs the digital modulation and demodulation and controls the external radio chip. This includes D/A and A/D conversion. The PHY can operate in each of the following three ISM bands: 2.4, 5.2 and 5.8 GHz. Within each of these bands three non-overlapping channels are available. The PHY facilitates seamless switching between each of the channels and bands, dynamically optimizing the RF footprint for the actual wireless environment.

The USB2.0 PHY and controller are directly connected to the Audio function block to ensure the seamless flow of audio and bulk data. The USB controller is directly controlled by the microcontroller.

The microcontroller of the DARR83 integrates an 8052 MCU as well as an 8 kbytes data RAM, 1 kbyte of program ROM and 45 kbytes program RAM. The MCU is used to configure and monitor the wireless audio core processes.

The Control I/O function block is used for serial communication and incorporates a UART as well as an I^2C master and slave interface. The I^2C master interface is used when the DARR83 is the controlling device in the application. If the DARR83 is controlled by an other host controller, the I^2C slave interface is used.

The Peripherals and Clock function block contains the supporting functions for the chip and includes a crystal oscillator, clock generator, power management unit, auxiliary ADC, RC clock oscillator, General Purpose I/O and a voltage regulator.

Block Diagram

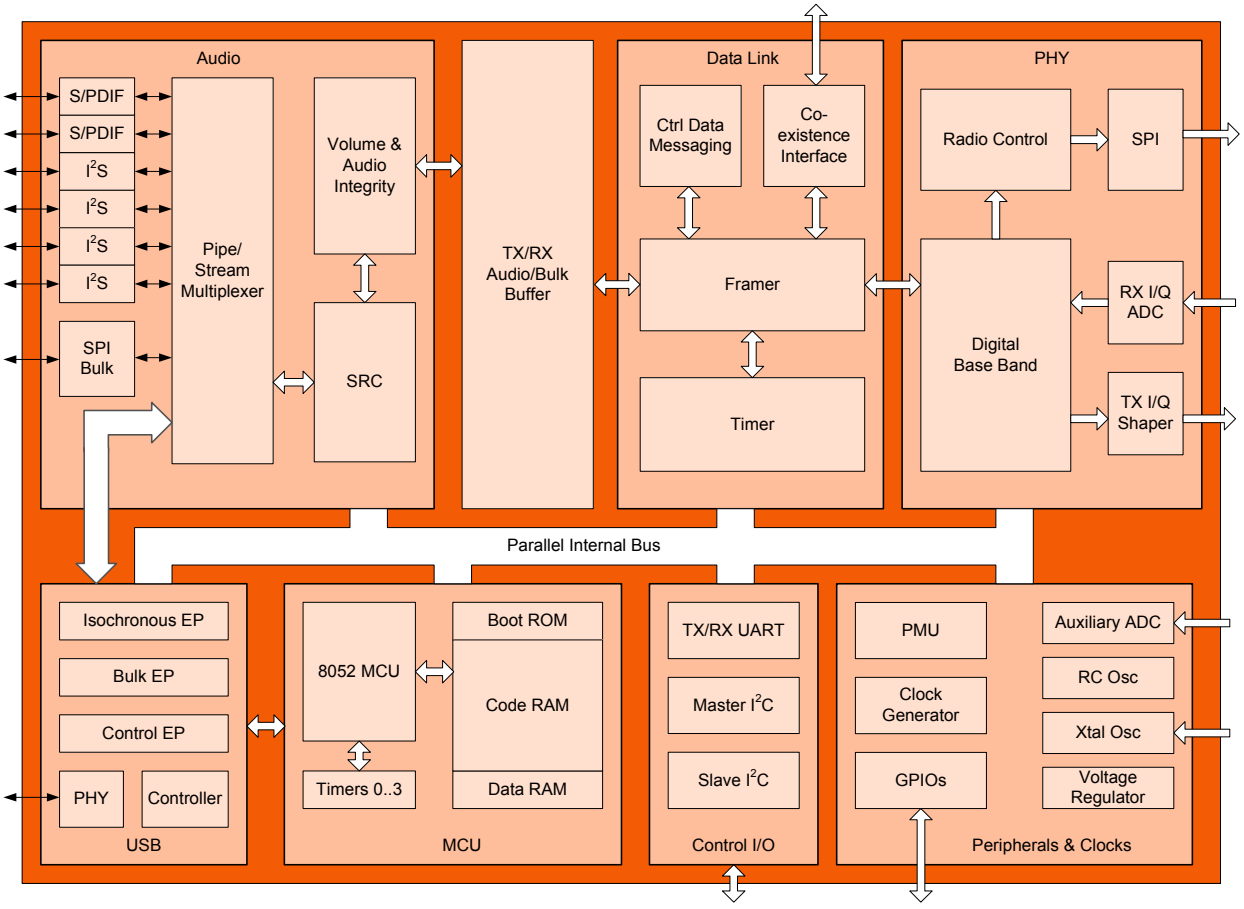

Figure 1 Internal Block Diagram

PRODUCT PREVIEW

Package Outline

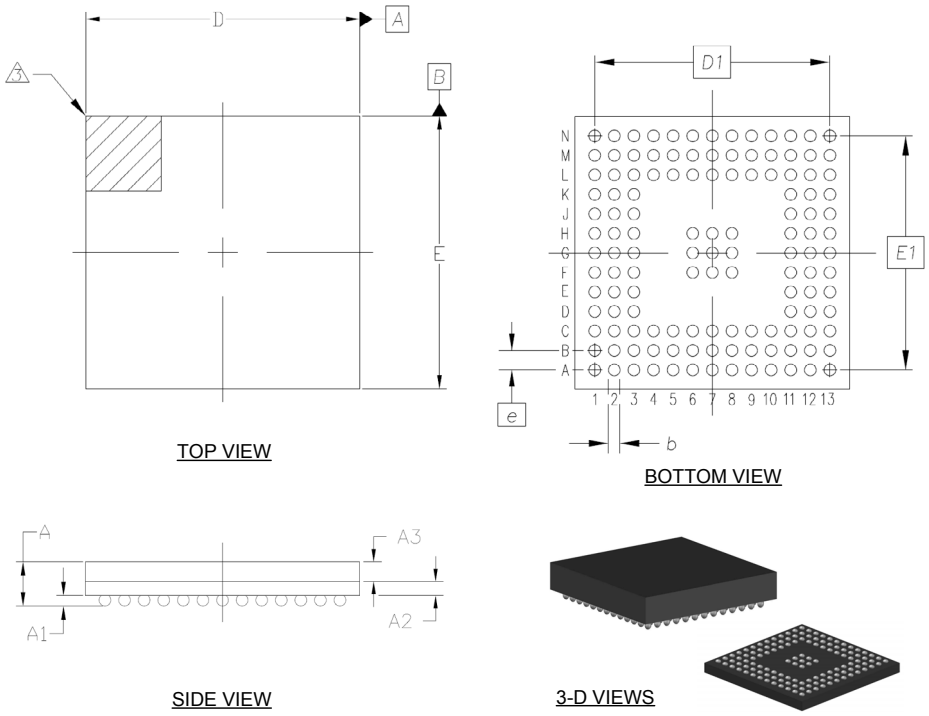

Figure 2 129-FBGA Package Definition

Table 1 129-FBGA Dimensions

	MILLIMETER			INCH		
SYMBOL	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.99	1.10	1.21	.039	.043	.048
A1	0.20	0.24	0.28	.008	.009	.011
A2	0.32	0.36	0.40	.013	.014	.016
A3	0.47	0.50	0.53	.019	.020	.021
b	0.25	0.30	0.35	.010	.012	.014
D	6.90	7.00	7.10	.272	.276	.280
D1		6.00 BSC			.236 BSC	
E	6.90	7.00	7.10	.272	.276	.280
E1		6.00 BSC			.236 BSC	
e		0.50 BSC			.197 BSC	
f	0.40	0.50	0.60	.016	.020	.024

Notes:

1. Dimensions and tolerances per ASME Y14.5M-1994
2. Controlling dimensions are in mm.
3. Details of A1 corners are optional and may consist of ink dot, laser mark or metallized marking, but must be located within the zone indicated.
4. Solder balls are normally a tin lead solder or lead free solder.
5. Refer to JEDEC Outline MO-195 for datums. Features and dimensions are not shown.
6. Primary datum C and seating place are defined by the spherical crowns of the solder balls.