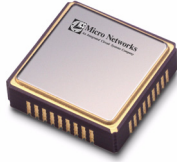




## GENERAL DESCRIPTION

The M2006-03 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for frequency translation and jitter attenuation of a master reference clock in a cable modem termination system (CMTS). External loop filter components allow tailoring of the PLL loop response.



The M2006-03 includes a phase-slope limiting feature to prevent disruptive output clock phase changes upon input reference reselection.

## FEATURES

- ◆ Integrated SAW (surface acoustic wave) delay line
- ◆ VCSO center frequency of 491.52MHz
- ◆ Jitter 9ps rms, typical, over 100Hz to 12kHz  
Jitter 3ps rms, typical, over 12kHz to 1GHz
- ◆ PLL phase slope limiter circuit
- ◆ Single-ended reference inputs support LVCMOS, LVTTTL
- ◆ All output clocks are differential LVPECL compatible
- ◆ Two downstream clocks, frequency-selectable
- ◆ One upstream clock, frequency-selectable
- ◆ REF\_OUT always provides a 10.24MHz reference clock
- ◆ All output rising edges aligned to within 1nsec of selected input reference rising edge (unless M2\_SEL= 1)
- ◆ Output duty cycle 47-53% worst case
- ◆ Single 3.3V power supply
- ◆ Small 9 x 9 mm SMT (surface mount) package

## PIN ASSIGNMENT (9 x 9 mm SMT)

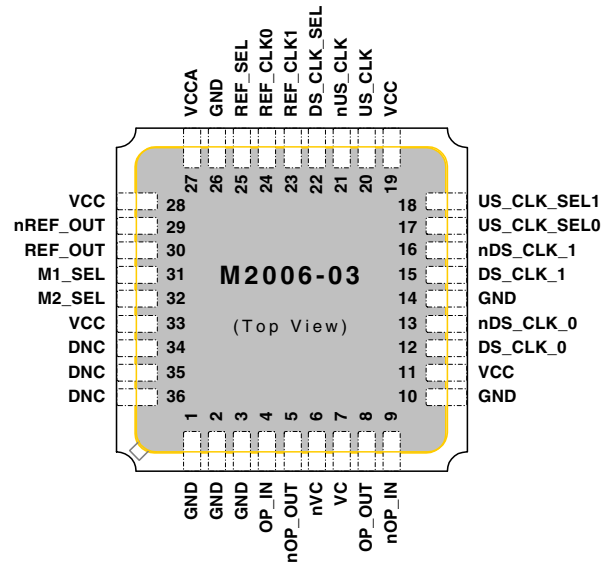


Figure 1: Pin Assignment

## Selectable Frequencies (MHz) for M2006-03-491.5200

Input Ref. Clock:	2.048, 4.096, 10.24, or 20.48 MHz
VCSO Frequency:	491.52 MHz
Downstream Clock:	245.76 or 491.52 MHz
Upstream Clock:	40.96, 81.92, 163.84, or 491.52 MHz
Output Ref. Clock:	10.24 MHz

Table 1: Selectable Frequencies (MHz) for M2006-03-491.5200

## SIMPLIFIED BLOCK DIAGRAM

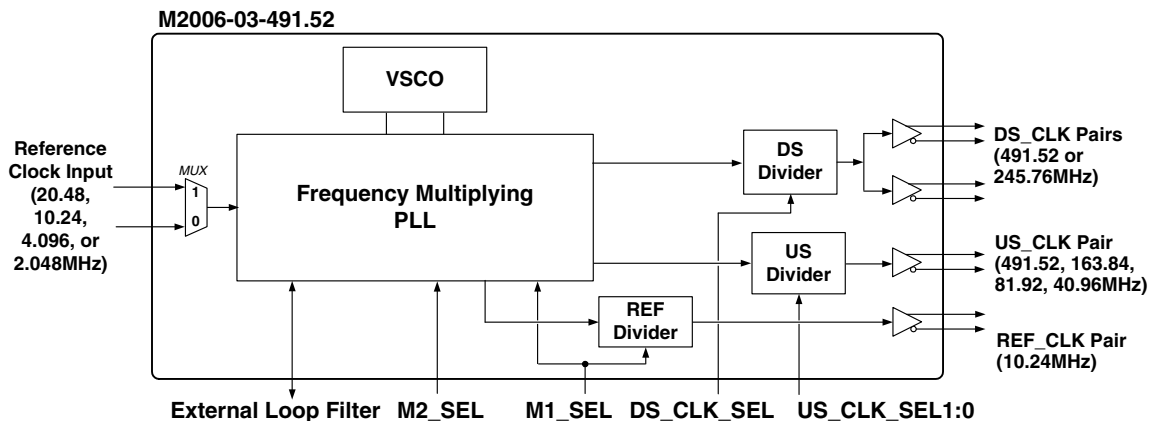


Figure 2: Simplified Block Diagram





## FUNCTIONAL DESCRIPTION

The M2006-03 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks.

An internal high "Q" SAW filter provides low jitter signal performance and controls the output frequency of the VCISO (Voltage Controlled SAW Oscillator). The VCISO center frequency is an integer multiple of the input reference frequency.

The M2006-03 is available with a 491.52MHz VCISO frequency that is specifically designed to support DOCSIS modem applications. As such, the M2006-03-491.520 (see "Ordering Information" on pg. 6) accepts input reference frequencies of: 2.048, 4.096, 10.24, and 20.48MHz.

### Input Reference

The selectable reference inputs are applied to the REF\_CLK1 and REF\_CLK0 input pins as necessary.

The REF\_SEL pin selects the reference input:

- REF\_SEL = 1 selects REF\_CLK1.
- REF\_SEL = 0 selects REF\_CLK0.

The selected reference clock is supplied directly to the phase detector of the PLL.

### The PLL

The PLL (Phase Locked Loop) includes the phase detector, the VCISO, and two feedback dividers (labeled "M1 Divider" and "M2 Divider").

The product of the two feedback divider values equals the overall feedback divider value "M".

$$M1 \times M2 = M$$

The M1\_SEL and M2\_SEL pins select the individual M1 and M2 divider values and, taken in combination, the overall feedback divider value ("M").

M2_SEL	M1_SEL	M2 Value	M1 Value	Overall Feedback Divider "M" Value
1	1	5	48	240
1	0		24	120
0	1	1	48	48
0	0		24	24

Table 3: Combined Feedback Divider Selectors and Values

"M" is used to divide the VCISO frequency so that it matches the input reference frequency. The relationship between the VCISO frequency, the M Divider, and the input reference frequency is:

$$F_{vciso} \div M = F_{ref\_in}$$

For the M2006-03-491.5200, which has a VCISO frequency of 491.52MHz, the four feedback divider values enable use with these corresponding input reference frequencies:

M2006-03-491.5200 VCISO Frequency (MHz)	M Feedback Divider Value	M2006-03-491.5200 Input Reference Frequency (MHz)
491.52	240	2.048
	120	4.096
	48	10.24
	24	20.48

Table 4: Feedback Divider Values and Input Reference Frequencies

Because both inputs to the phase detector have the same frequency, the PLL can control the VCISO to keep it locked to the input reference clock.

### Post-PLL Dividers

The M2006-03 also features three post-PLL dividers: the downstream ("DS") divider, the upstream ("US") divider, and the output reference ("REF") divider.

**The DS Divider:** Divides the VCISO frequency to produce one of two downstream output frequencies (1/2 or 1/1 of the VCISO frequency). The DS\_CLK\_SEL pin determines the DS Divider value.

DS_CLK_SEL	DS Value	M2006-03-491.5200 Downstream Output Frequencies (MHz)
1	2	245.76
0	1	491.52

Table 5: Downstream Divider Selector, Values, and Frequencies

**The US Divider:** Divides the VCISO frequency to produce one of four upstream output frequencies (1/12, 1/6, 1/3 or 1/1 of the VCISO frequency). The US\_CLK\_SEL1 and US\_CLK\_SEL0 pins determine the US Divider value.

US_CLK_SEL1	US_CLK_SEL0	US Value	M2006-03-491.5200 Upstream Output Frequencies (MHz)
1	1	12	40.96
1	0	6	81.92
0	1	3	163.84
0	0	1	491.52

Table 6: Upstream Divider Selectors, Values, and Frequencies

**The REF Divider:** Used along with the M1 divider value to ensure that the output system reference clock always equals the VCISO frequency divided by 48. The M1\_SEL pin determines the REF Divider value.

M1_SEL	REF Value	M2006-03-491.5200 VCISO Frequency (MHz)	M1 Value	REF Value	M2006-03-491.5200 REF Output Frequency (MHz)
1	1	491.52	48	1	10.24
0	2		24	2	

Table 7: M1 Selector and REF Divider Values and Frequencies



## Outputs

The M2006-03 provides a total of four differential LVPECL output pairs:

- **Downstream** - The selected frequency is output from DS\_CLK\_0 and from DS\_CLK\_1.
- **Upstream** - The selected frequency is output from US\_CLK.
- **System reference** - The 10.24MHz clock is output from REF\_OUT.

## External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2006-03 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 4).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

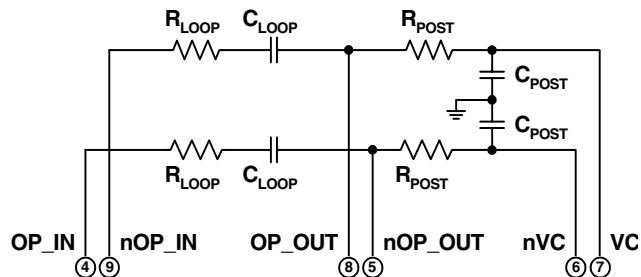


Figure 4: External Loop Filter

## External Loop Filter Component Values for M2006-03-491.520

Input Ref. Clock Freq.	PLL Bandwidth	Damping Factor	R loop	C loop	R post	C post
20.48MHz	1kHz	1.6	9.1kΩ	0.22μF	20kΩ	250pF
10.24MHz	1kHz	2.7	20kΩ	0.22μF	20kΩ	250pF
4.096MHz	1kHz	2.0	50kΩ	0.047μF	20kΩ	250pF
2.048MHz	1kHz	2.7	100kΩ	0.047μF	20kΩ	250pF

Table 8: External Loop Filter Component Values for M2006-03-491.520

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Symbol	Parameter	Rating	Unit
V <sub>I</sub>	Inputs	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>O</sub>	Outputs	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>CC</sub>	Power Supply Voltage	4.6	V
T <sub>S</sub>	Storage Temperature	-45 to +100	°C

Table 9: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Positive Supply Voltage	3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Operating Temperature	0		+70	°C

Table 10: Recommended Conditions of Operation



## ELECTRICAL SPECIFICATIONS FOR M2006-03-491.520

### DC Characteristics

Unless stated otherwise,  $V_{CC} = 3.3 \text{ Volts} \pm 5\%^1$ ,  $T_A = 0^\circ\text{C} \text{ to } 70^\circ\text{C}$ , VCSO Frequency = 491.52MHz, Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$

	Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
Power Supply	$V_{CC}$ <sup>1</sup>	Positive Supply		3.135	3.3	3.465	V	$V_{CC} = V_{CCA} = 3.3V$
	$I_{CC}$	Power Supply Current			162		mA	
All Inputs	$V_{IH}$	Input High Voltage	REF_SEL,	2		$V_{CC} + 0.3$	V	
	$V_{IL}$	Input Low Voltage	M1_SEL, M2_SEL,	-0.3		0.8	V	
	$I_{IH}$	Input High Current	US_CLK_SEL0,			150	$\mu\text{A}$	
			US_CLK_SEL1,					
	$I_{IL}$	Input Low Current	DS_CLK_SEL,	-5			$\mu\text{A}$	
	$C_{in}$	Input Capacitance	REF_CLK0, REF_CLK1			4	pF	
Pull-down	$R_{pull\downarrow}$	Internal Pull-down Resistor	(All Inputs)		51		k $\Omega$	
Differential Outputs	$V_{OH}$	Output High Voltage	US_CLK, nUS_CLK,	$V_{CC} - 1.4$		$V_{CC} - 1.0$	V	
			DS_CLK_0, nDS_CLK_0,					
	$V_{OL}$	Output Low Voltage	DS_CLK_1, nDS_CLK_1,	$V_{CC} - 2.0$		$V_{CC} - 1.7$	V	
	$V_{P-P}$	Peak to Peak Output	REF_OUT, nREF_OUT	0.6		0.85	V	

Note 1:  $V_{CC}$  applies to both VCC and VCCA pins (i.e.,  $V_{CC} = V_{CCA} = 3.3V$ )

Table 11: DC Characteristics

### AC Characteristics

Unless stated otherwise,  $V_{CC} = 3.3 \text{ Volts} \pm 5\%^1$ ,  $T_A = 0^\circ\text{C} \text{ to } 70^\circ\text{C}$ , VCSO Frequency = 491.52MHz, Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$

	Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions
Input Frequency Range	$F_{IN}$	Input Frequency	REF_CLK0, REF_CLK1		20.48		MHz	M2_SEL=0, M1_SEL=0
					10.24		MHz	M2_SEL=0, M1_SEL=1
					4.096		MHz	M2_SEL=1, M1_SEL=0
					2.048		MHz	M2_SEL=1, M1_SEL=1
Output Frequency Range	$F_{DS\_OUT}$	Downstream Output Frequency Range	DS_CLK_0, nDS_CLK_0,		491.52		MHz	DS_CLK_SEL=0
			DS_CLK_1, nDS_CLK_1		245.76		MHz	DS_CLK_SEL=1
	$F_{US\_OUT}$	Upstream Output Frequency Range	US_CLK, nUS_CLK		491.52		MHz	US_CLK_SEL1:0=00
					163.84		MHz	US_CLK_SEL1:0=01
					81.92		MHz	US_CLK_SEL1:0=10
				40.96		MHz	US_CLK_SEL1:0=11	
	$F_{REF\_OUT}$	Reference Output	REF_OUT, nREF_OUT		10.24		MHz	
	APR	VCSO Pull-Range		$\pm 100$	$\pm 150$		ppm	
	$\Phi_n$	Single Side Band Phase Noise @491.52MHz	1kHz Offset		-72		dBc/Hz	
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms)	Non-deterministic		9		ps	100Hz to 12kHz
					3		ps	12kHz to 1GHz
	$t_{PW}$	Output Duty Cycle, High Time <sup>2</sup>		47		53	%	
	$t_{LOCK}$	PLL Lock Time				100	ms	
	$t_R$	Output Rise Time <sup>2</sup>		325	450	500	ps	20% to 80%
	$t_F$	Output Fall Time <sup>2</sup>		325	450	500	ps	20% to 80%
	$t_S$	Input to Output Skew	Rising Edge			1	ns	

Note 1:  $V_{CC}$  applies to both VCC and VCCA pins (i.e.,  $V_{CC} = V_{CCA} = 3.3V$ )  
Note 2: See Parameter Measurement Information on pg. 6

Table 12: AC Characteristics



## PARAMETER MEASUREMENT INFORMATION

### Output Rise and Fall Time

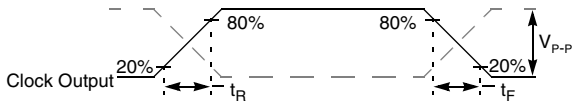


Figure 5: Output Rise and Fall Time

### Output Duty Cycle

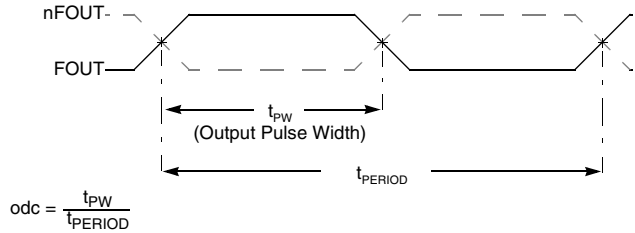
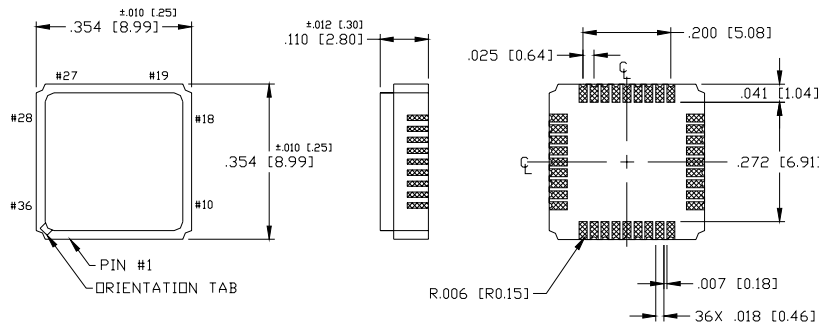


Figure 6: Output Duty Cycle

## DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

### Mechanical Dimensions:



Refer to the SAW PLL application notes web page at [www.icst.com/products/appnotes/SawPLLAppNotes.htm](http://www.icst.com/products/appnotes/SawPLLAppNotes.htm) for application notes, including recommended PCB footprint, solder mask, and furnace profile.

#### NOTES:

1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE  $\pm 0.005$  [0.13]

Figure 7: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

## ORDERING INFORMATION

For VCISO Frequency (MHz)	Order Part Number
491.52	M2006-03-491.5200

Table 13: Ordering Information

Other frequencies available upon request.

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