NB3N2302

3.3V / 5V 5MHz to 133MHz Frequency Multiplier and Zero Delay Buffer

ON Semiconductor®

http://onsemi.com

Description

The NB3N2302 is a versatile Zero Delay Buffer that operates from 5 MHz to 133 MHz with a 3.3 V or 5 V power supply. It accepts a reference input and drives a ÷1 and a ÷2 clock output. The NB3N2302 has an on−chip PLL which locks to the input reference clock presented on the REF_IN pin. The PLL feedback is required to be driven to the FBIN pin and can be obtained by connecting either the OUT1 or OUT2 pin to the FBIN pin.

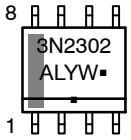
The Function Select inputs control the various multiplier output frequency combinations as shown in Table 1.

Features

- Output Frequency Range: 5 MHz to 133 MHz
- Two LVTTL/LVCMOS Outputs
- 65 ps Typical Jitter OUT2
- 115 ps Typical Jitter OUT1
- 25 ps Typical Output−to−Output Skew
- Operating Voltage Range: V_{DD} = 3.3 V ±5% or 5 V ±10%
- Clock Multiplication of the Reference Input Frequency, See Table 1 for Options
- Packaged in 8−Pin SOIC
- −40°C to +85°C Ambient Operating Temperature Range
- Ideal for PCI−X and Networking Clocks
- These are Pb−Free Devices

MARKING DIAGRAM

SOIC−8
D SUFFIX
CASE 751



2302	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

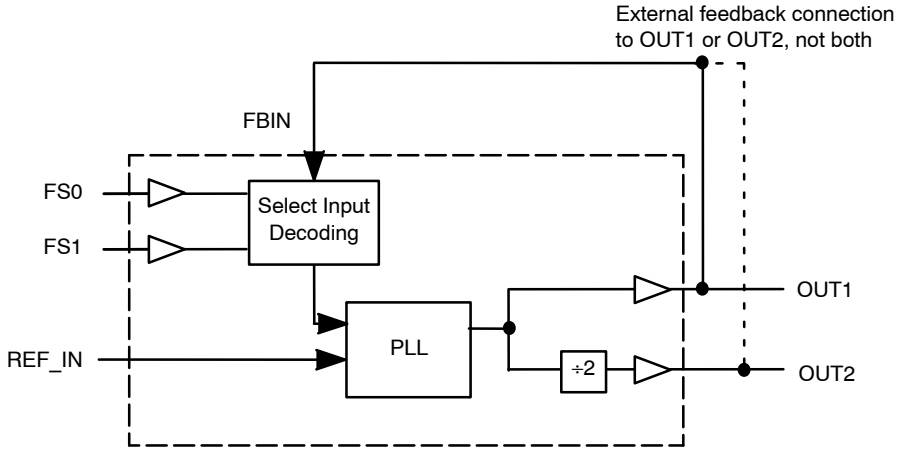


Figure 1. Simplified Logic Diagram

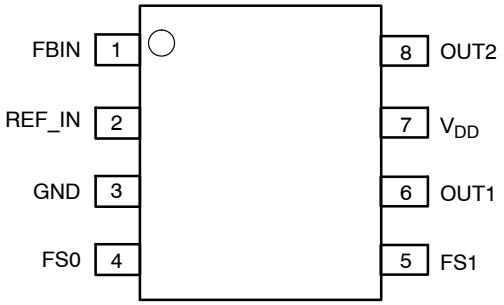


Figure 2. NB3N2302 Package Pinout (Top View) 8−pin SOIC (150 mil)

Table 1. CLOCK MULTIPLIER SELECT TABLE

FBIN	FS0	FS1	OUT1	OUT2	REF_IN Min (MHz)	REF_IN Max (MHz)
OUT1	0	0	2 x REF	REF	5	66.5
OUT1	1	0	4 x REF	2 x REF	5	33.25
OUT1	0	1	REF	REF / 2	10	133
OUT1	1	1	8 x REF	4 x REF	5	16.625
OUT2	0	0	4 x REF	2 x REF	5	33.25
OUT2	1	0	8 x REF	4 x REF	5	16.625
OUT2	0	1	2 x REF	REF	5	66.5
OUT2	1	1	16 x REF	8 x REF	5	8.3125

Table 2. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	FBIN	LVCMOS/LVTTL Input	Feedback Input: This input must be fed by one of the outputs (OUT1 or OUT2) to ensure proper functionality. If the trace between FBIN and the output pin being used for feedback is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations are synchronized to the REF signal input (REF_IN).
2	REF_IN	LVCMOS/LVTTL Input	Reference Input: The output signals are synchronized to this signal.
3	GND	Power	Negative supply voltage; Connect to ground, 0 V
4	FS0	LVCMOS/LVTTL Input	Function Select Input: Tie to V_{DD} (HIGH, 1) or GND (LOW, 0) as desired per Table 1.
5	FS1	LVCMOS/LVTTL Input	Function Select Input: Tie to V_{DD} (HIGH, 1) or GND (LOW, 0) as desired per Table 1.
6	OUT1	LVCMOS/LVTTL Output	Output 1: The frequency of the signal provided by this pin is determined by the feedback signal connected to FBIN, and the FS0:1 inputs (see Table 1).
7	VDD	Power	Positive supply voltage This pin should be bypassed with a 0.1 μF decoupling capacitor. Use ferrite beads to help reduce noise for optimal jitter performance.
8	OUT2	LVCMOS/LVTTL Output	Output 2: The frequency of the signal provided by this pin is one−half of the frequency of OUT1. See Table 1.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index	UL 94 V−O @ 0.125 in
Transistor Count		6910 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin	GND = 0 V		−0.5 to +7.0	V
T_A	Operating Temperature Range, Commercial Industrial			0 to +70 −40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
T_B	Ambient Temperature under Bias			−55 to +125	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−8 SOIC−8	190 130	°C/W
P_D	Power Dissipation			0.5	W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	SOIC−8	42	°C/W
T_{SOL}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power

Table 5. DC CHARACTERISTICS V_{DD} = 3.3 V ± 5% or 5 V ± 10%, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{DD}	Power Supply Current, 100 MHz, Unloaded Outputs V_{DD} = 3.3 V ± 5% V_{DD} = 5 V ± 10%		20 25	35 50	mA
V_{OH}	Output HIGH Voltage I_{OH} = −12 mA	2.4			V
V_{OL}	Output LOW Voltage I_{OL} = 12 mA			0.4	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V
I_{IH}	Input HIGH Current, V_{IN} = V_{DD}			5	μA
I_{IL}	Input LOW Current, V_{IN} = 0 V V_{DD} = 3.3 V ± 5% V_{DD} = 5 V ± 10%	−40 −80		5 5	μA

Table 6. AC CHARACTERISTICS V_{DD} = 3.3 V ± 5% or 5 V ± 10%, GND = 0 V, T_A = −40°C to +85°C (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{IN}	Input Frequency (Note 3)	5		133	MHz
f_{OUT}	Output Frequency, OUT1 15 pF load	10		133	MHz
t_D	Output Duty Cycle @ 1.4 V, 120 MHz, 50% duty cycle in, 15 pF load	40	50	60	%
t_r/t_f	Output rise and fall times; 0.8 V to 2.0V, 15 pF load V_{DD} = 3.3 V ± 5% V_{DD} = 5 V ± 10%			3.5 / 2.5 2.5 / 1.5	ns
t_{INCLK} t_r/t_f	Input Clock rise and fall time (Note 4)			10	ns
t_{LOCK}	PLL Lock Time, power supply stable			1.0	ms
t_{JC}	Cycle−to−cycle Jitter OUT1, f_{OUT} > 30 MHz OUT2, f_{OUT} > 30 MHz		115 65	300 300	ps
t_{DC}	Die “Fave Away” Out Time. 33 MHz reference input suddenly stopped (0 MHz). Number of cycles provided prior to output falling to < 16 MHz.	100			Clock Cycles
t_{pd}	Propagation Delay, (Note 10)	−350		350	ps
t_{skew}	Output−to−output skew; (Note 6)		25	250	ps

3. Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration). See Table 1.
4. Longer input rise and fall time degrades skew and jitter performance.
5. All AC specifications are measured with a 50 Ω transmission line, load terminated with 50 Ω to 1.4 V.
6. Skew is measured at 1.4 V on rising edges, all outputs with equal loading.
7. Duty cycle is measured at 1.4 V.
8. 33 MHz reference input suddenly stopped (0 MHz). Number of cycles provided prior to output falling to < 16 MHz.
9. Duty Cycle measured at 120 MHz. For 133 MHz, degrades to 35/65 worst case.
10. While in lock, propagation delay is measured from REF_IN to OUT1 using < 1 in feedback trace, (See Figure 1).

Overview

The NB3N2302 is a two−output zero delay buffer and frequency multiplier. It provides an external feedback path allowing maximum flexibility when implementing the Zero Delay feature. This is explained further in the sections of this datasheet titled “How to Implement Zero Delay,” and “Inserting Other Devices in Feedback Path.”

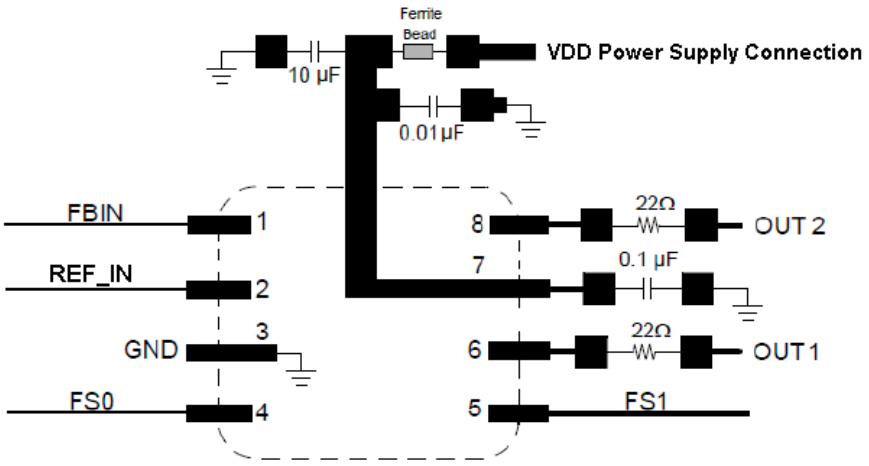


Figure 3. Schematic / Suggested Layout

How to Implement Zero Delay

Typically, Zero Delay Buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described as follows.

External feedback is the trait that allows for this compensation. The PLL on the ZDB causes the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feedback and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be implemented by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) that is put into the feedback path.

Referring to Figure 4, if the traces between the ASIC/Buffer and the destination of the clock signal(s) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device is driven HIGH at the same time when the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay from the ZDB output to the ASIC/Buffer output must be accounted for.

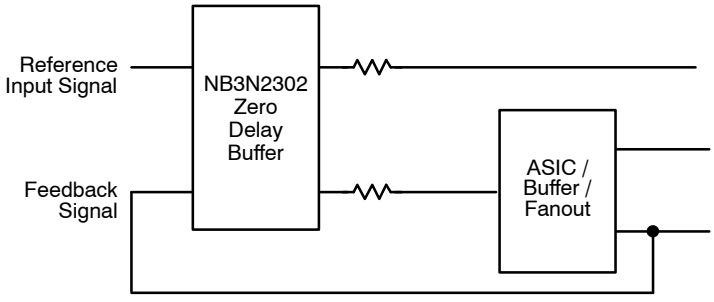
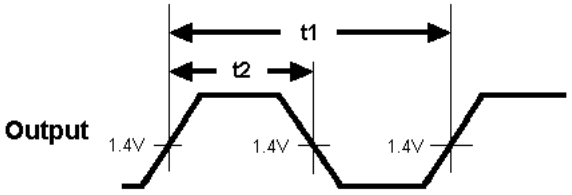


Figure 4. Output Buffer in the Feedback Path

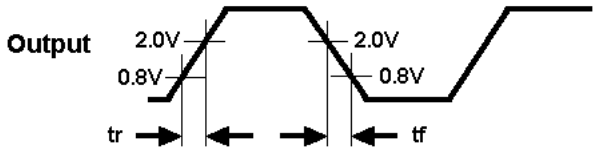
Phase Alignment

In cases where OUT1 (i.e., the higher frequency output) is connected to FBIN input pin the output OUT2 rising edges may be either 0° or 180° phase aligned to the IN input waveform (as set randomly when the input and/or power is supplied). If OUT2 is desired to be rising−edge aligned to the IN input's rising edge, then connect the OUT2 (i.e., the lowest frequency output) to the FBIN pin. This set−up provides a consistent input−output phase relationship.

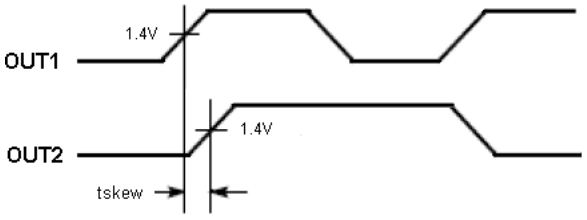
Output Duty Cycle



Output Rise and Fall Times



Output - Output Skew



Input - Output Propagation Delay

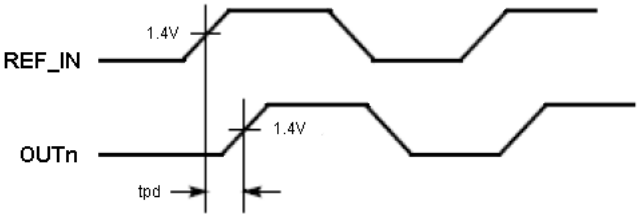


Figure 5. Switching Waveforms

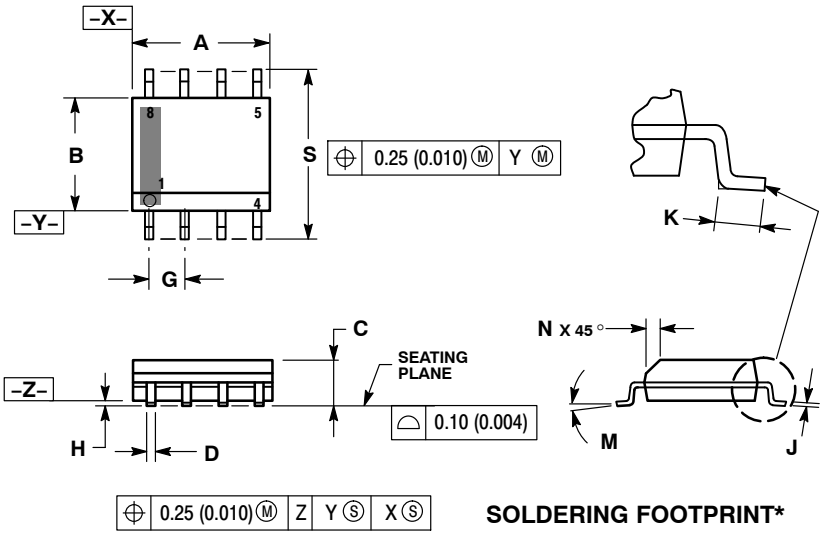
ORDERING INFORMATION

Device	Package	Shipping†
NB3N2302DG	SOIC−8 (Pb−Free)	98 Units / Rail
NB3N2302DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

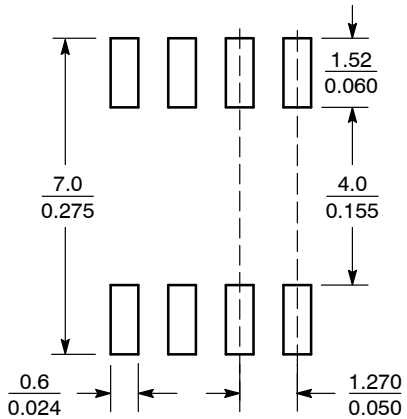
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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